

Point Curvature: Large Aspect Ratio: Small (≑1)

FIG. 1A PRIOR ART



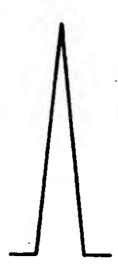
Point Curvature: Little Small Aspect Ratio: Small (≠4.5)

FIG. 1B PRIOR ART



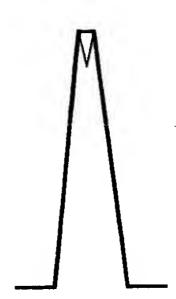
Point Curvature: Little Small Aspect Ratio: Small (≑1)

FIG. 1C PRIOR ART



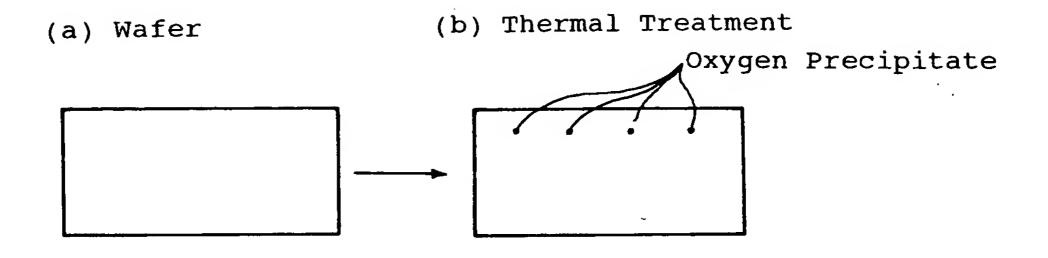
Point Curvature: Small (Several nm)
Aspect Ratio: Large (=10)

FIG. 1D PRESENT INVENTION



Point Curvature: Small (Several nm)
Aspect Ratio: Large (=10)

FIG. 1E PRESENT INVENTION



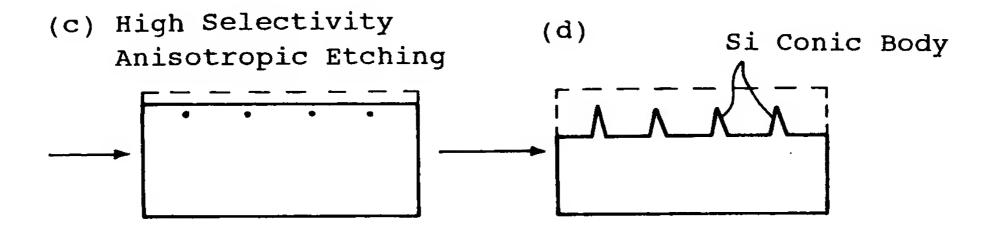
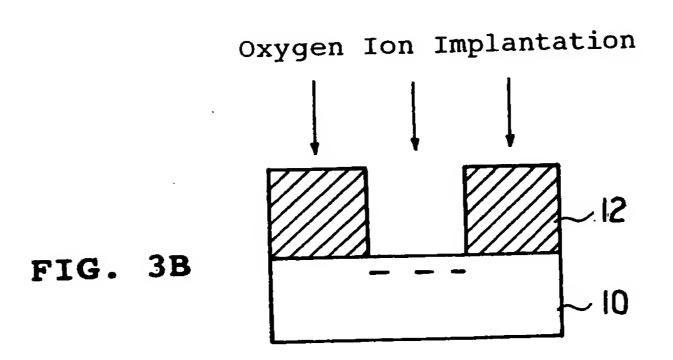
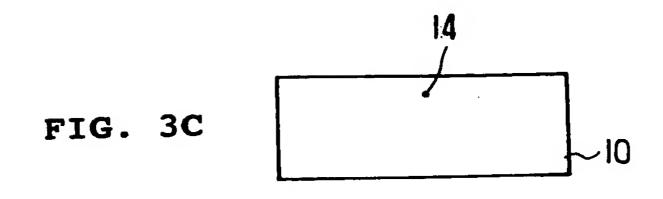
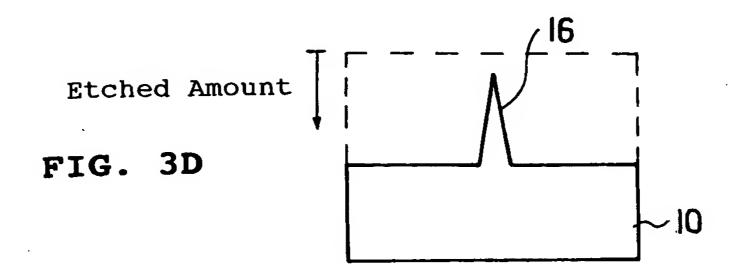


FIG. 2









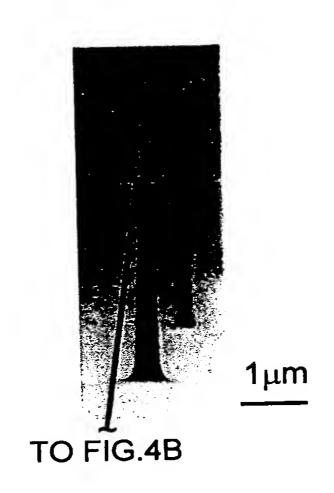


FIG.4A

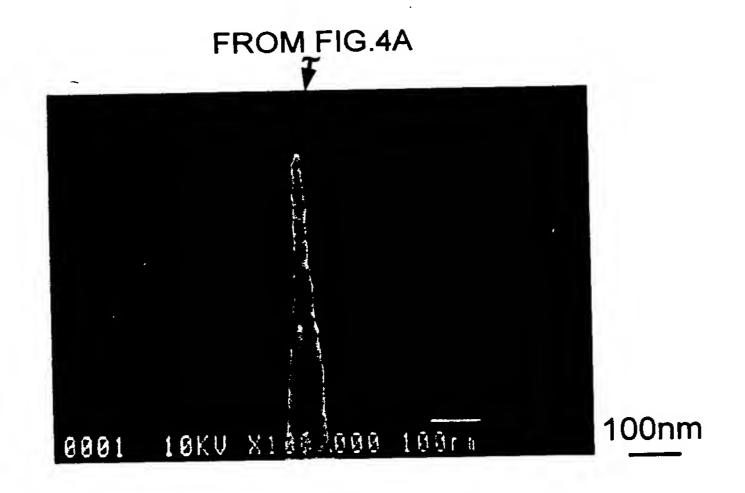


FIG.4B

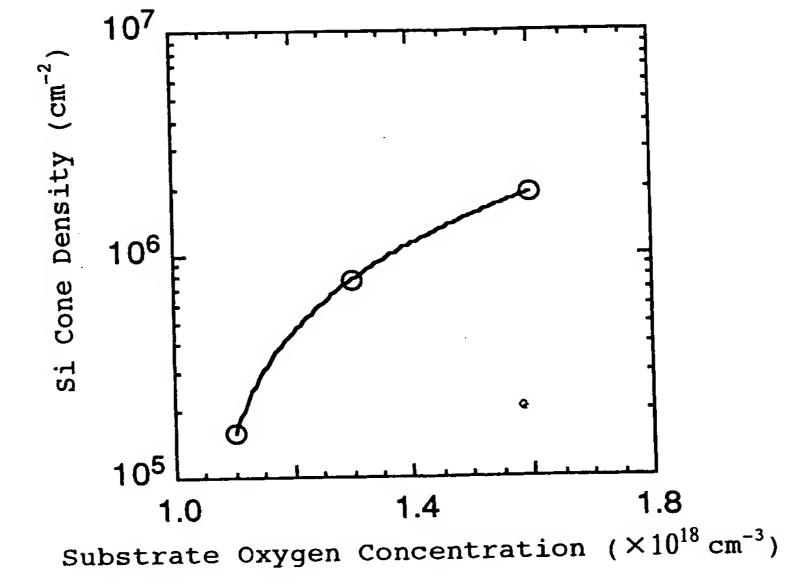


FIG. 5

B Implantation Amount:

7 X 10¹³cm⁻²

100μm

FIG.6A

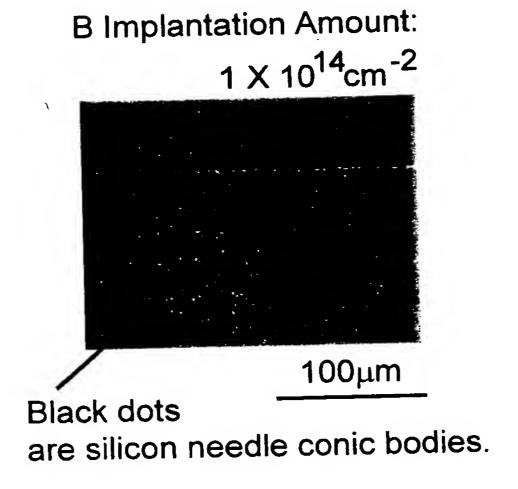
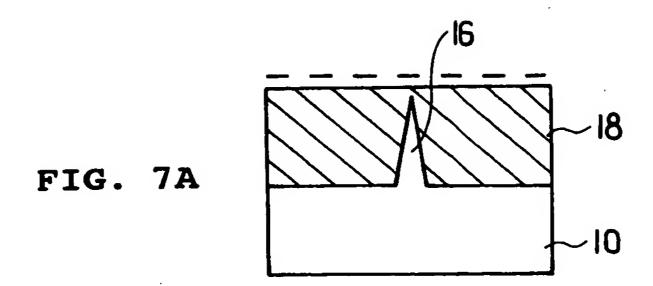
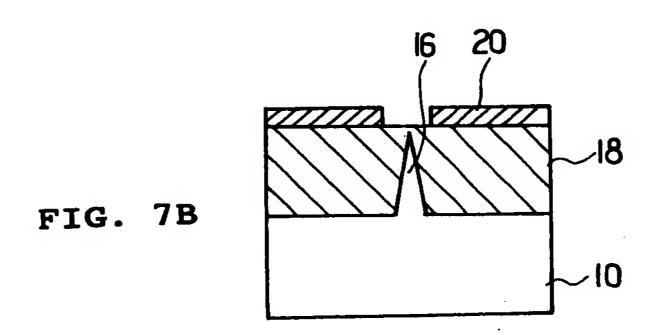
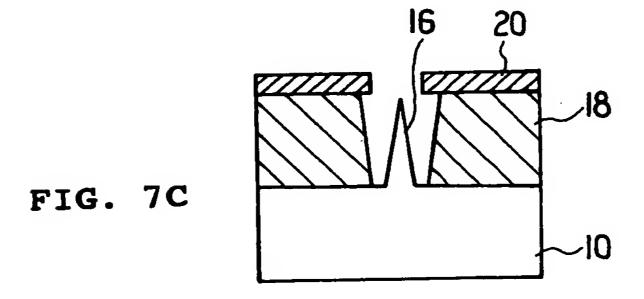
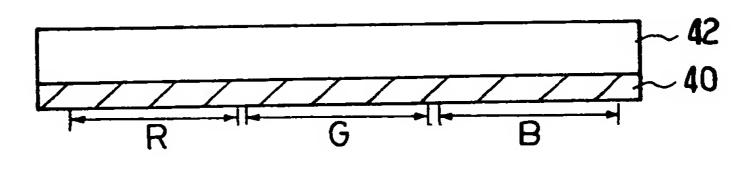


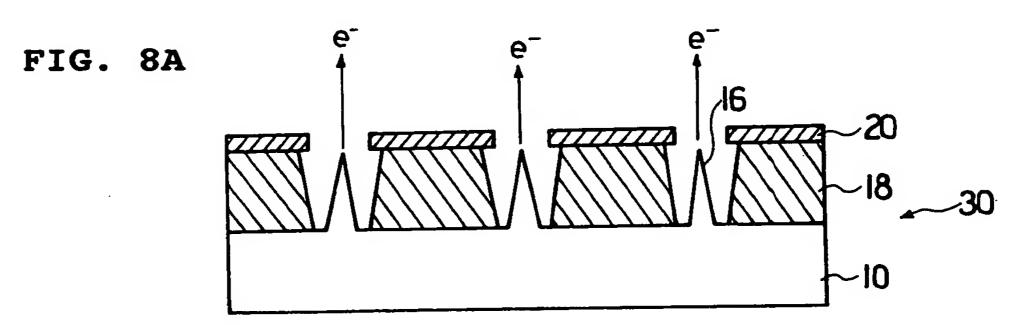
FIG.6B

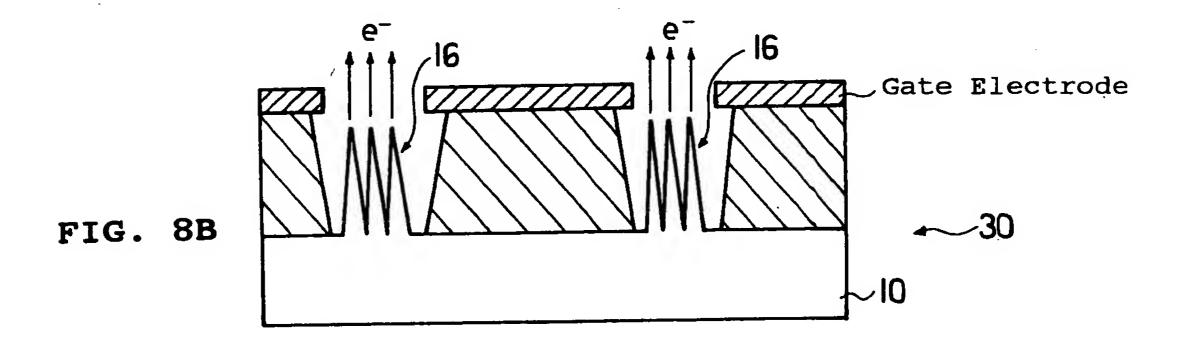












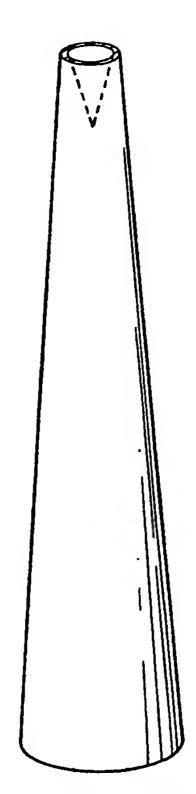


FIG. 9A

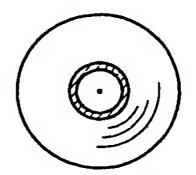
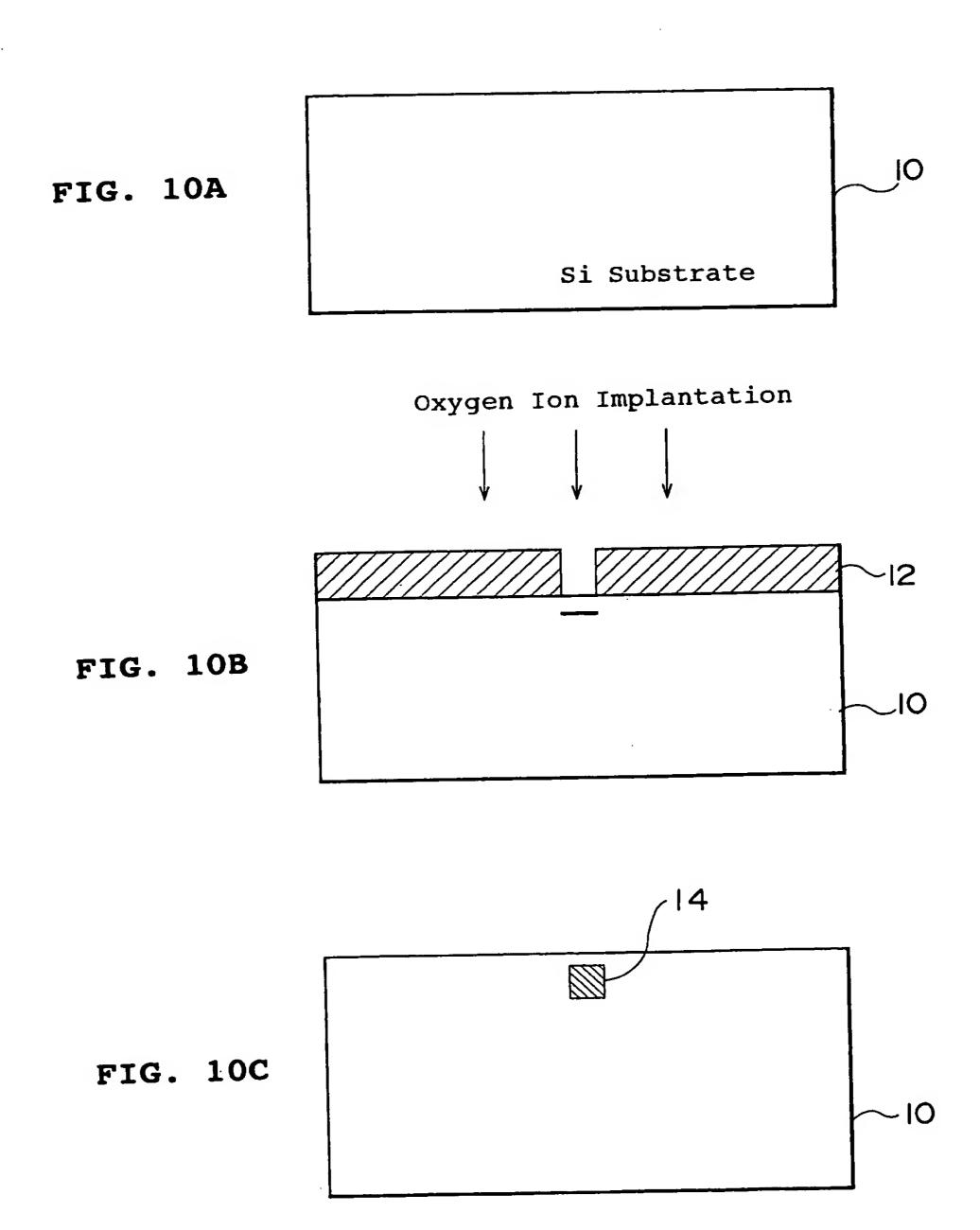
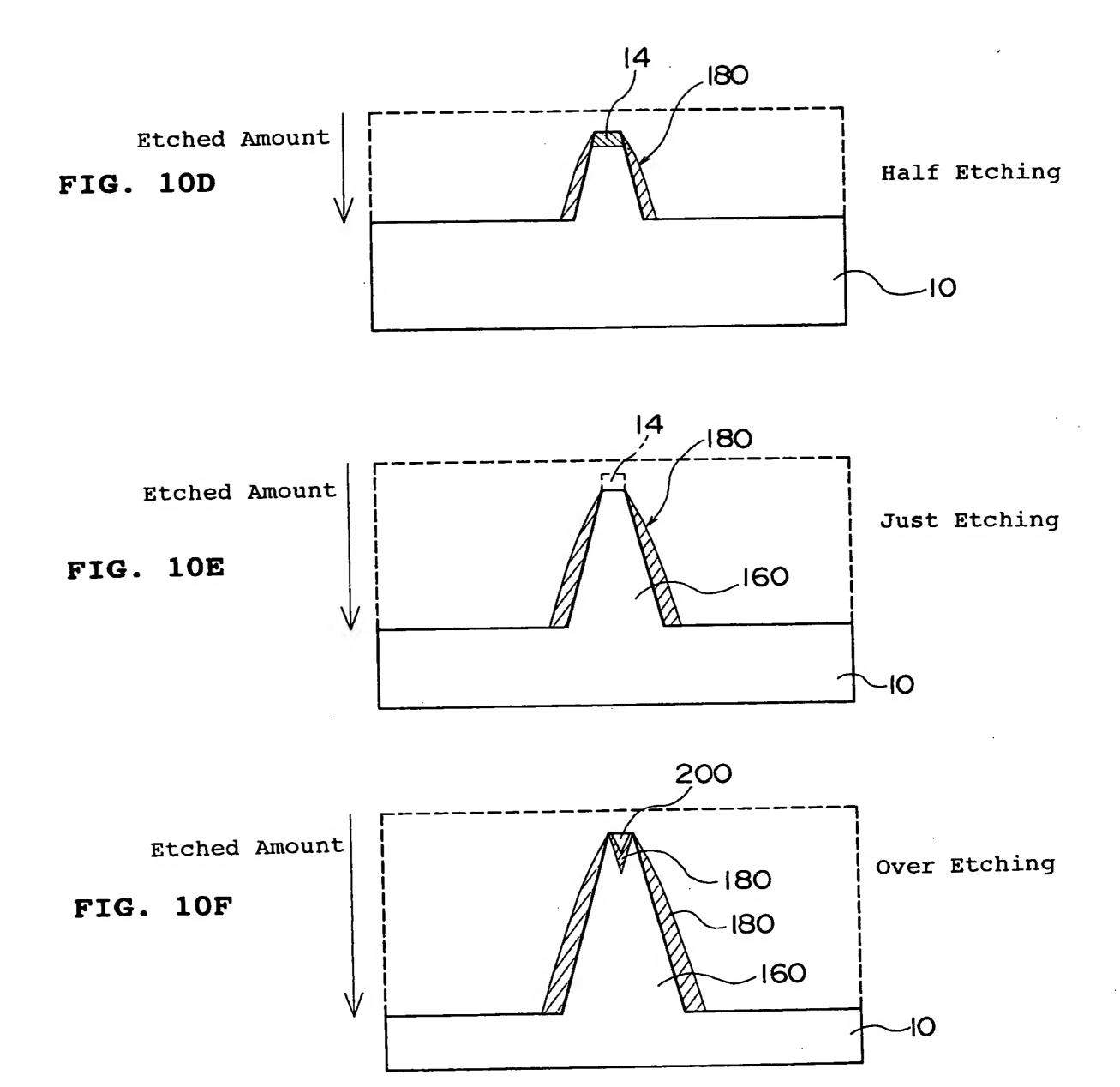


FIG. 9B





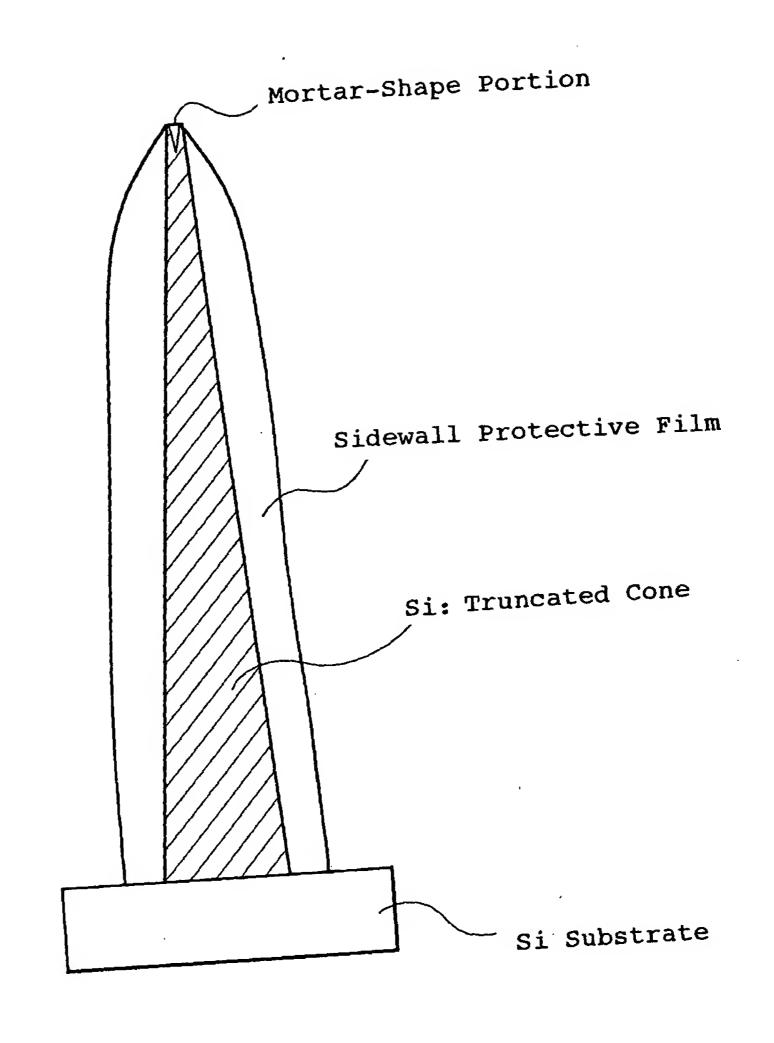
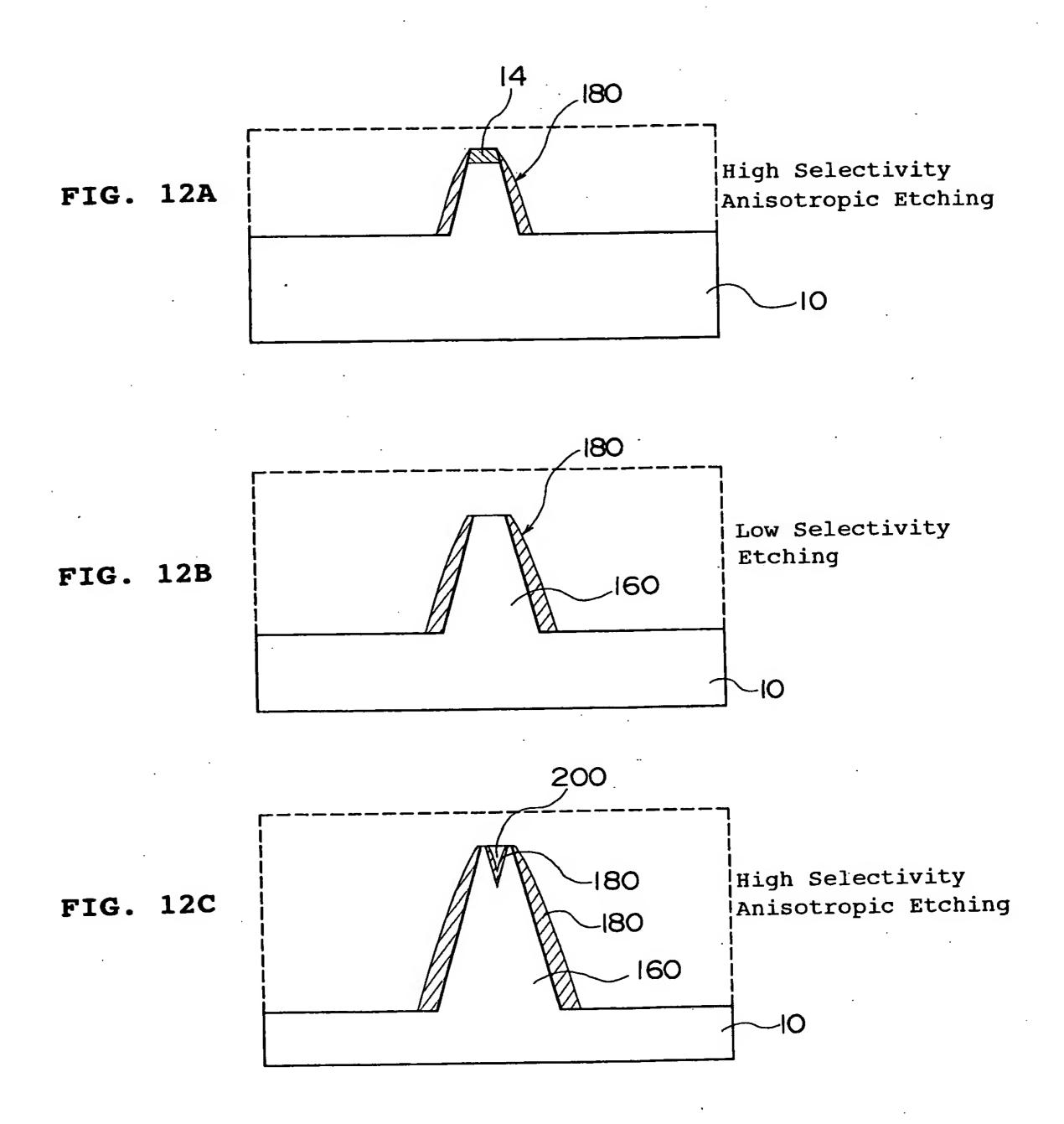
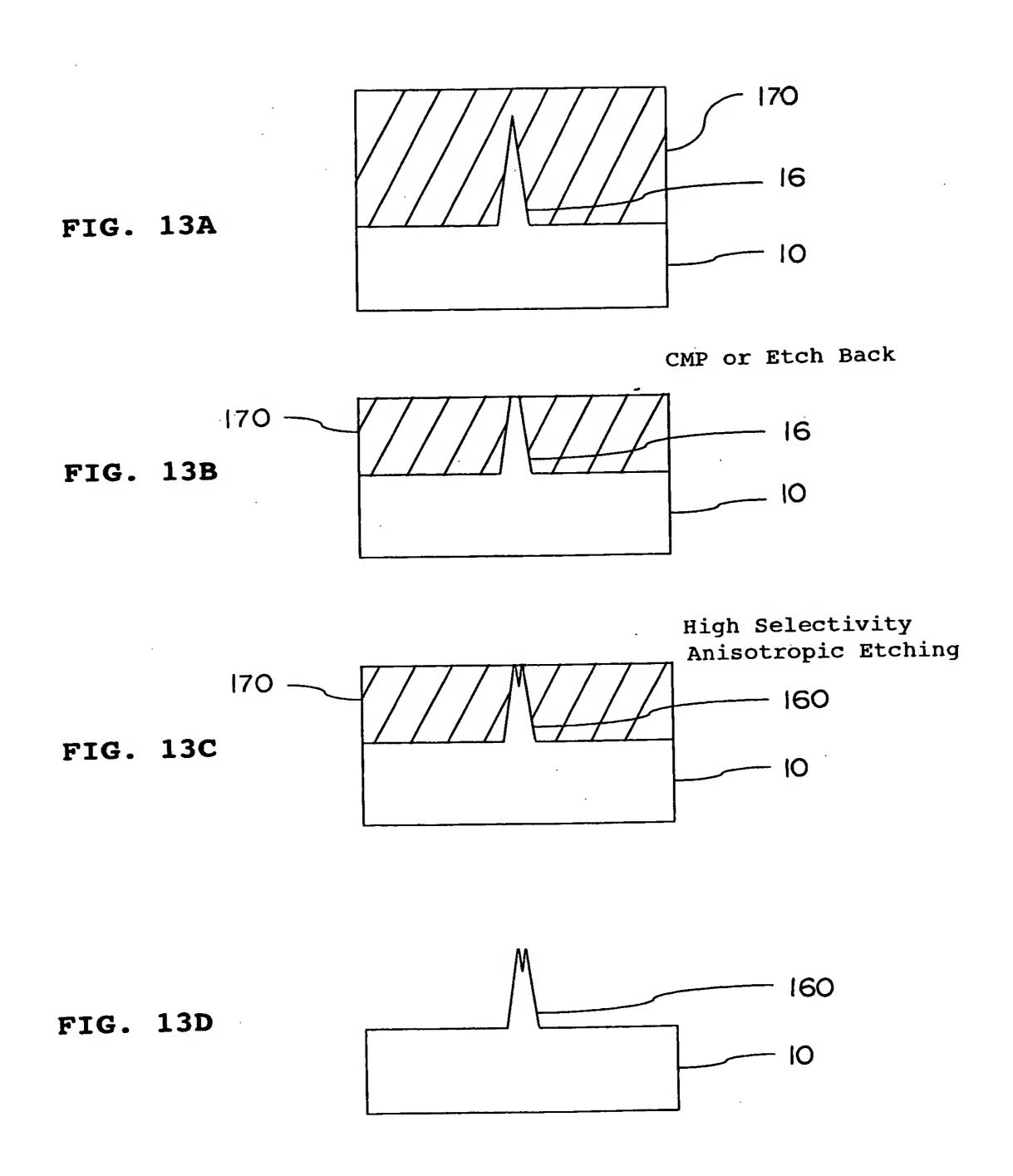


FIG. 11





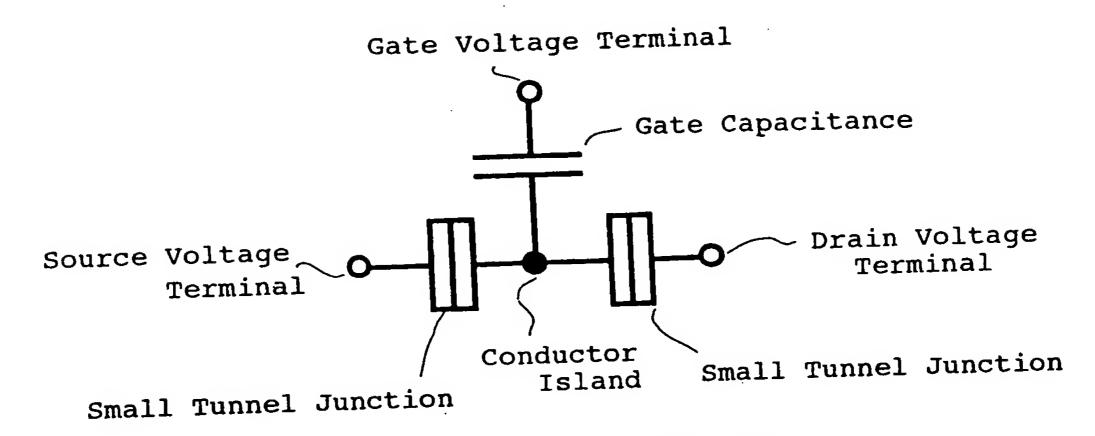


FIG. 14A PRIOR ART

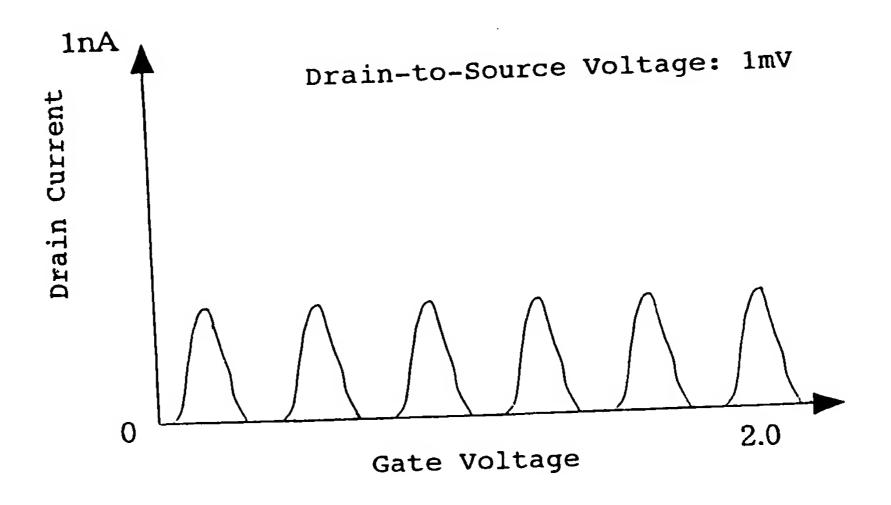


FIG. 14B PRIOR ART

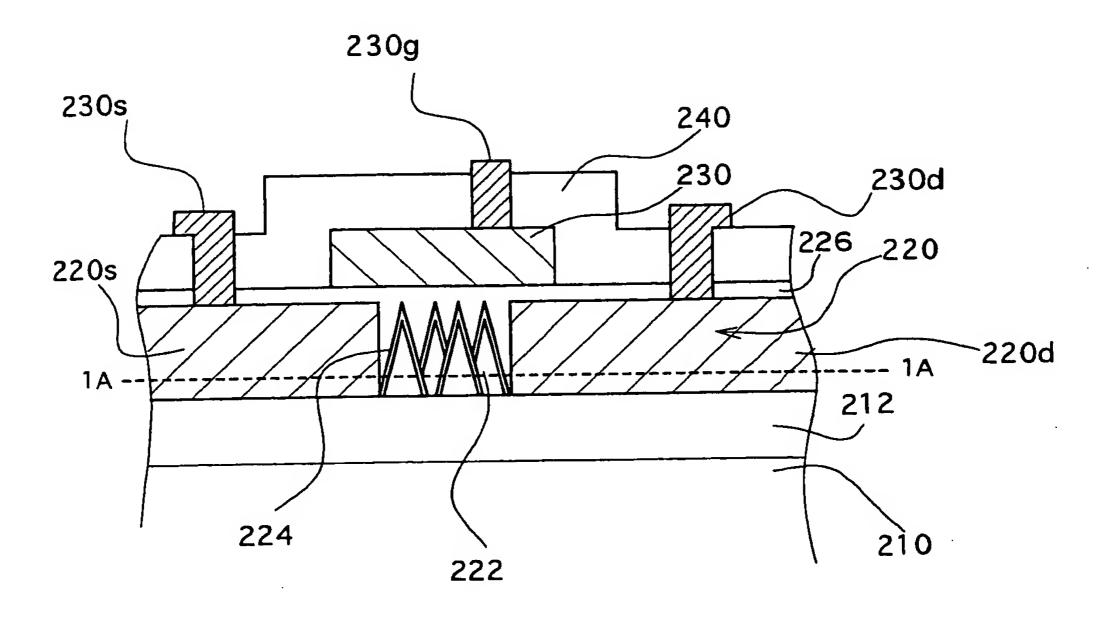


FIG. 15A

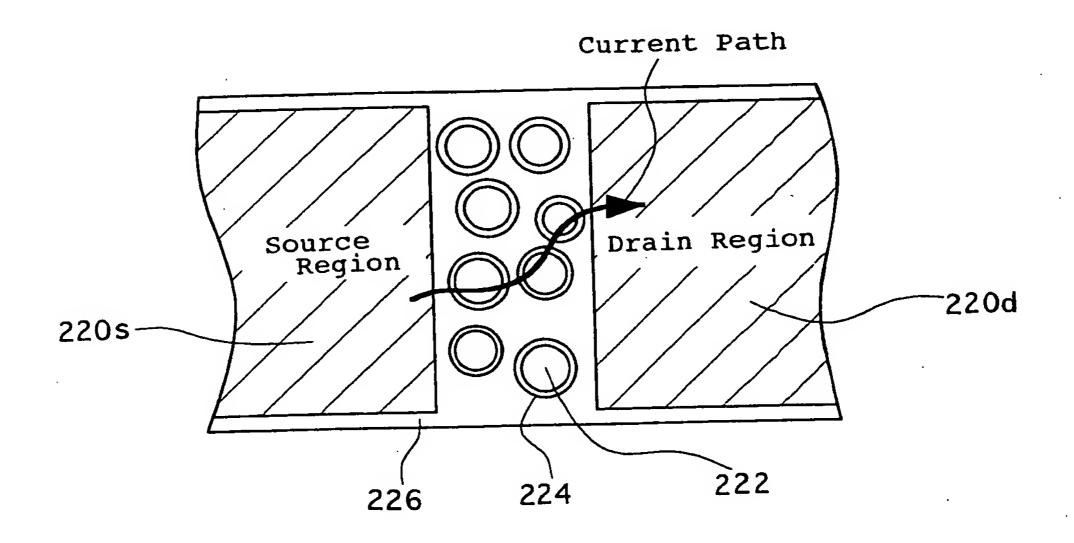
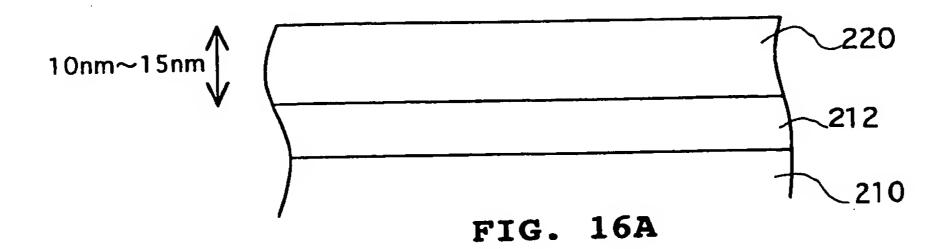
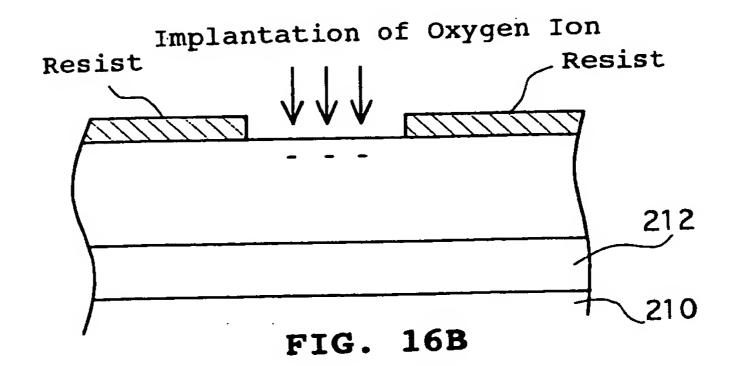
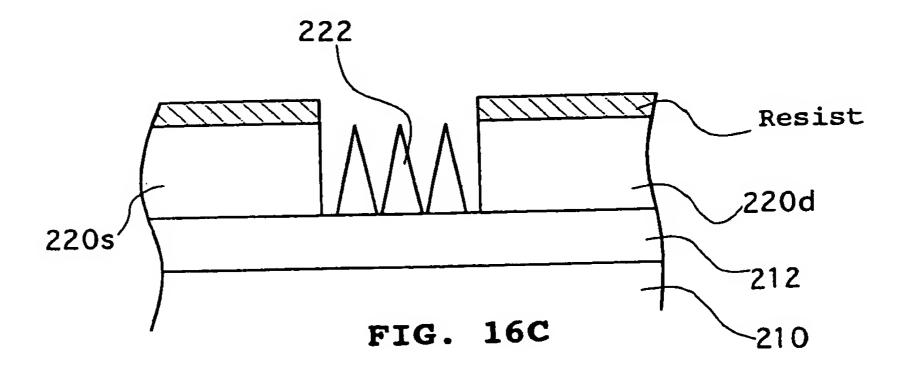
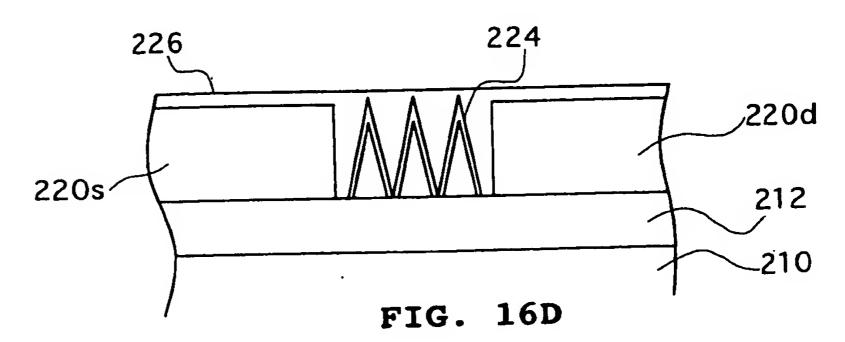


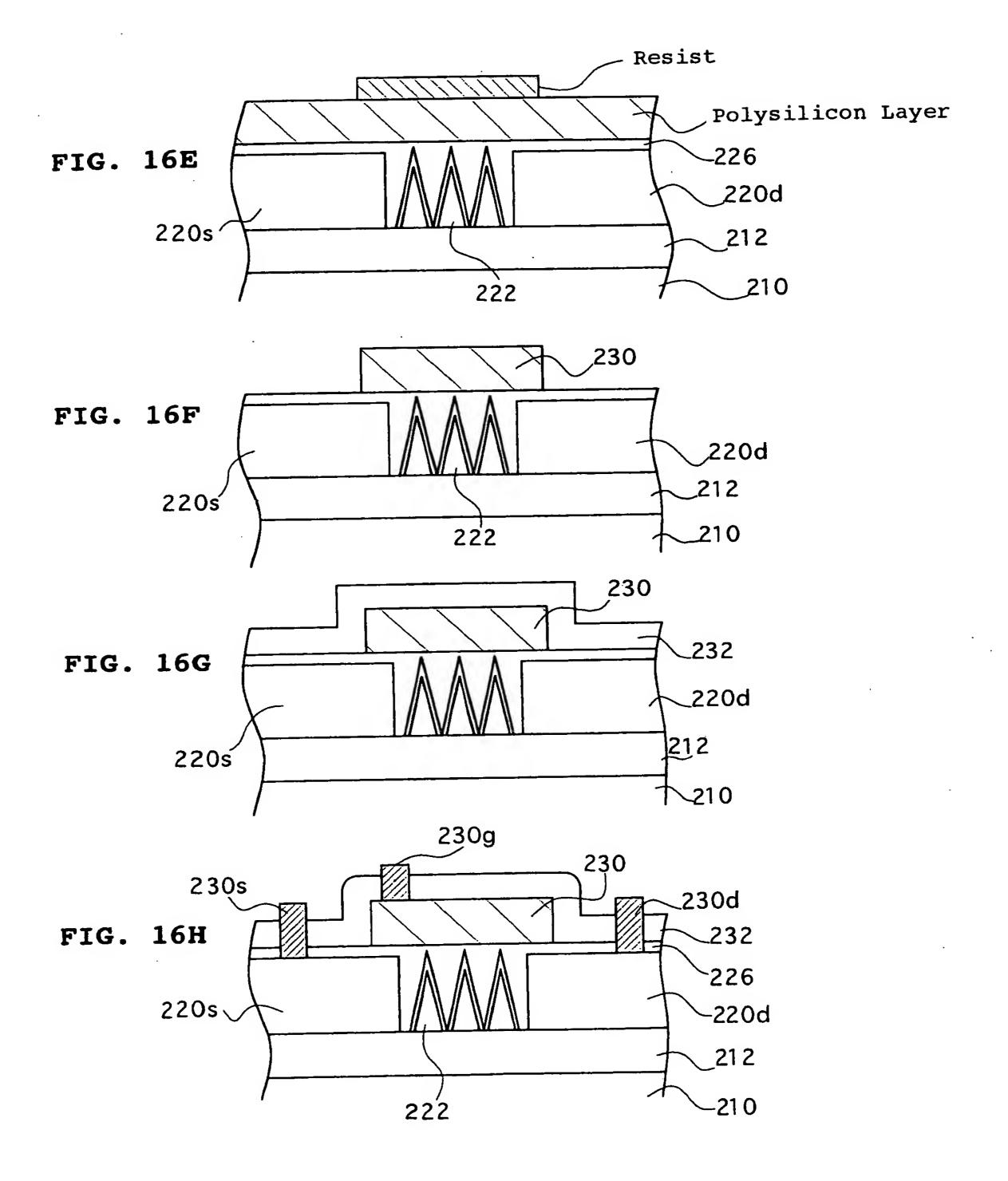
FIG. 15B

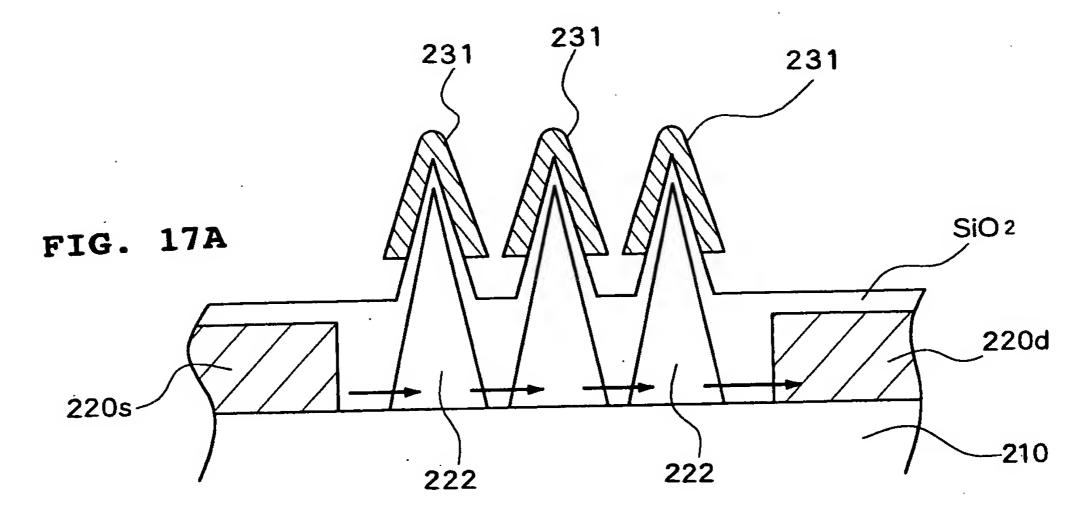




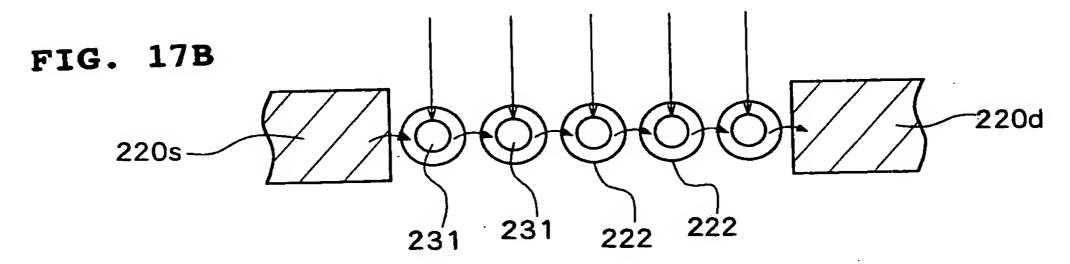


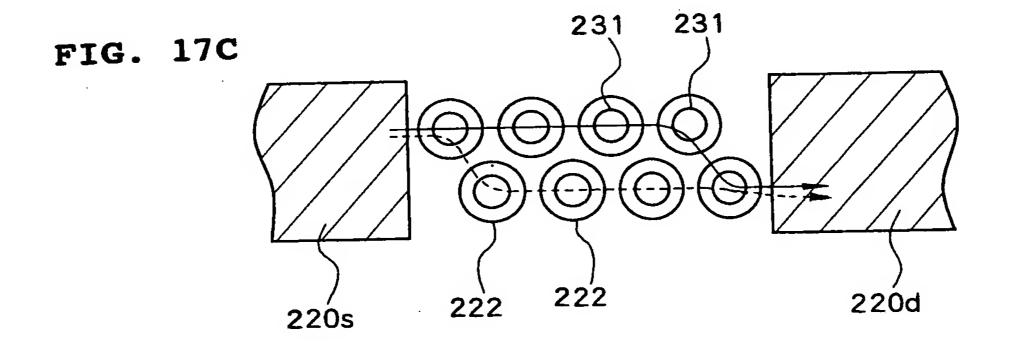






Selective Gate Control





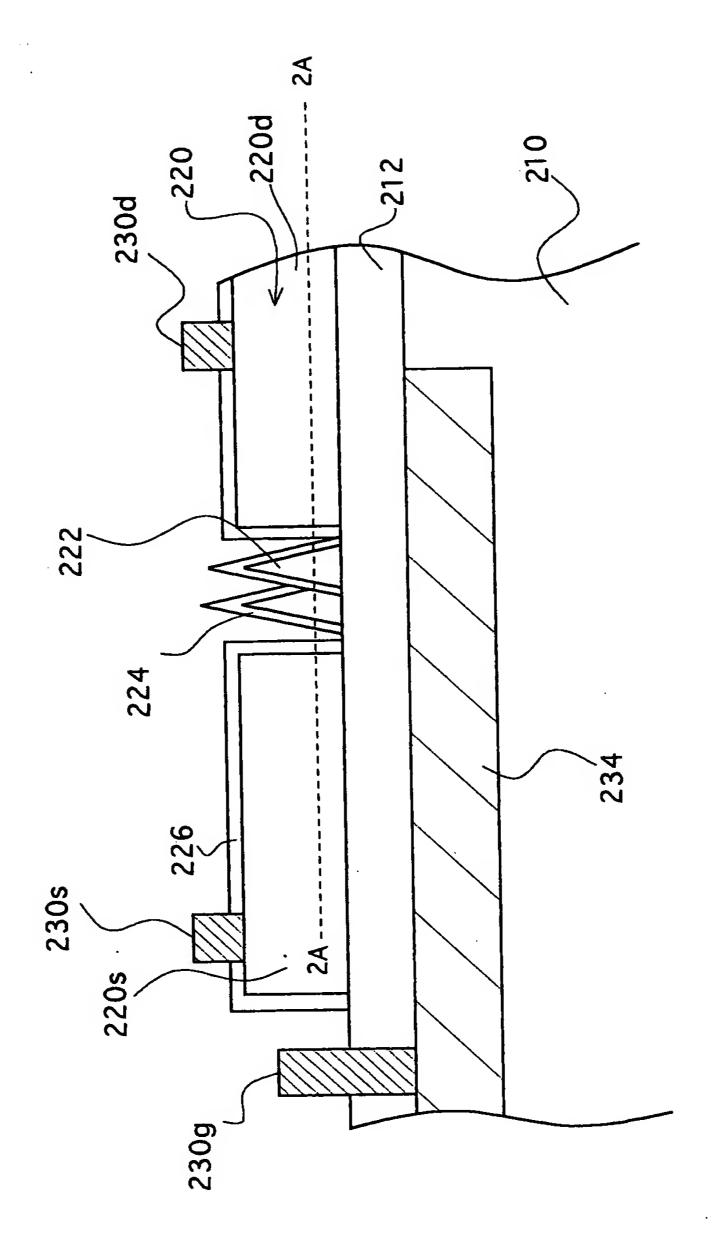


FIG. 18

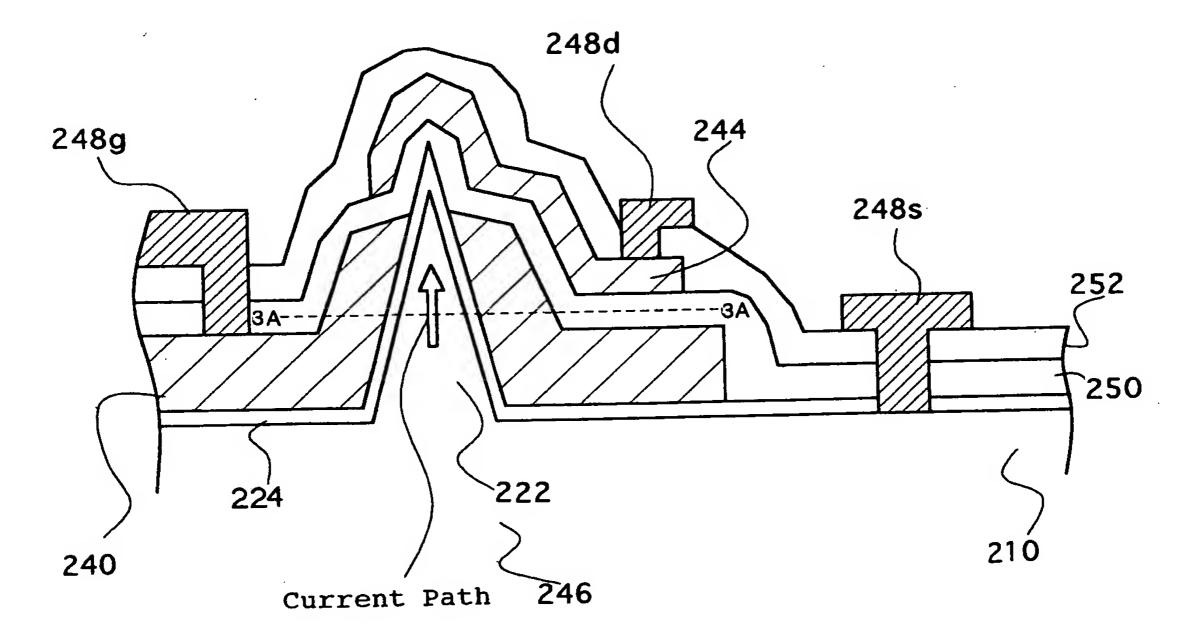


FIG. 19A

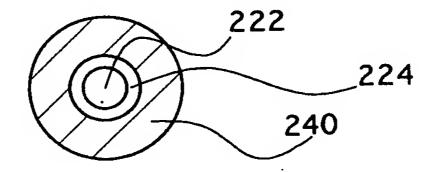
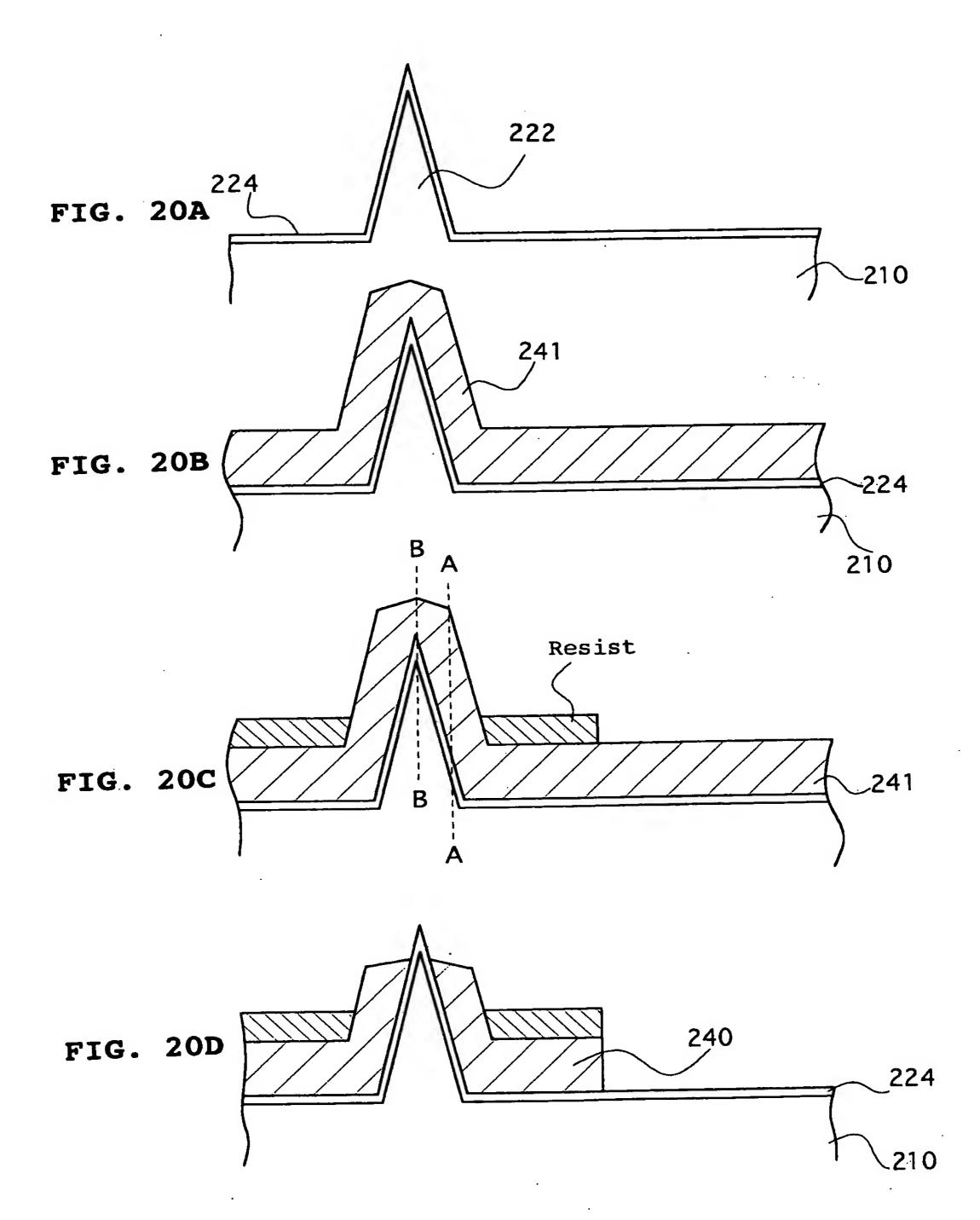
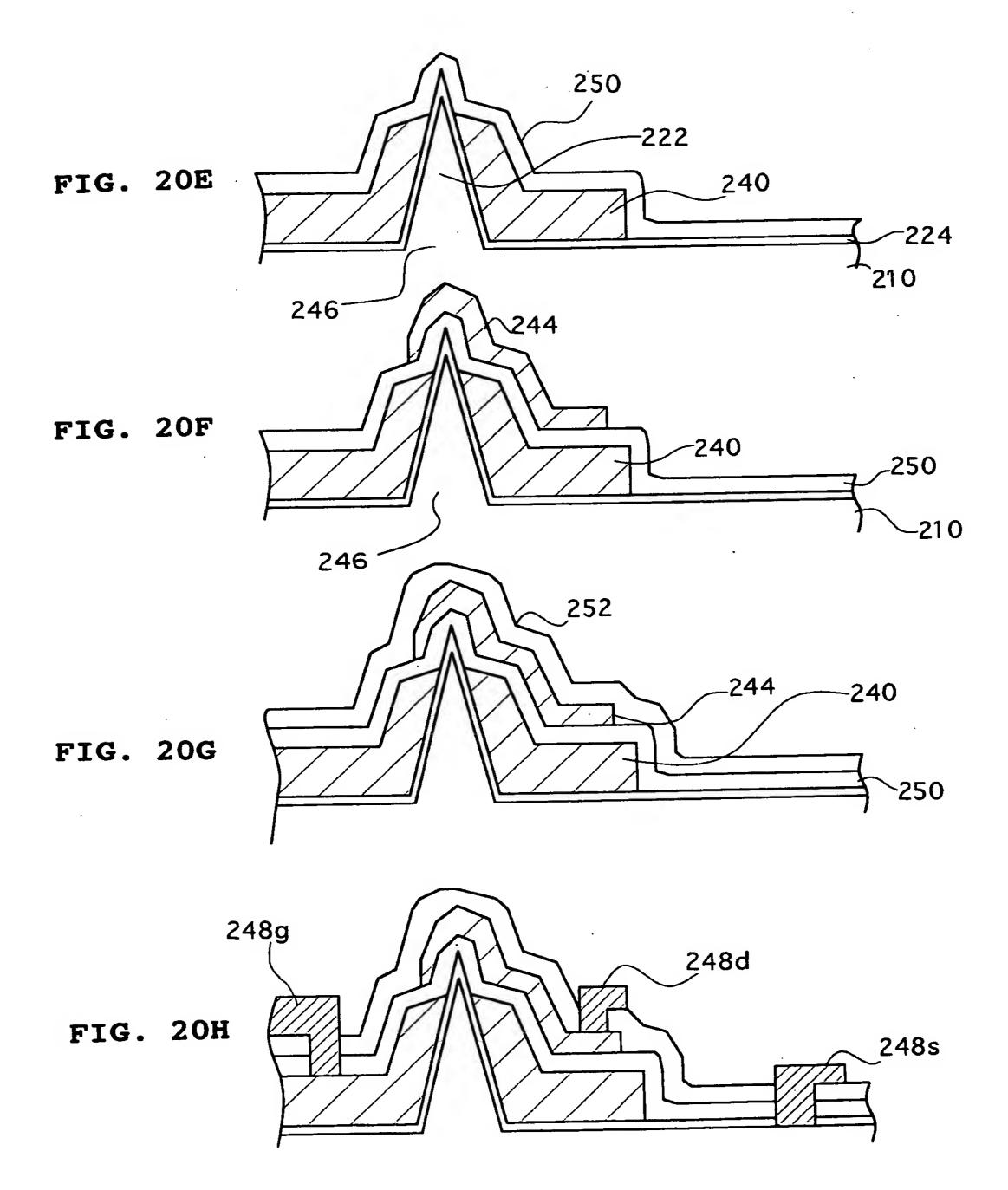


FIG. 19B





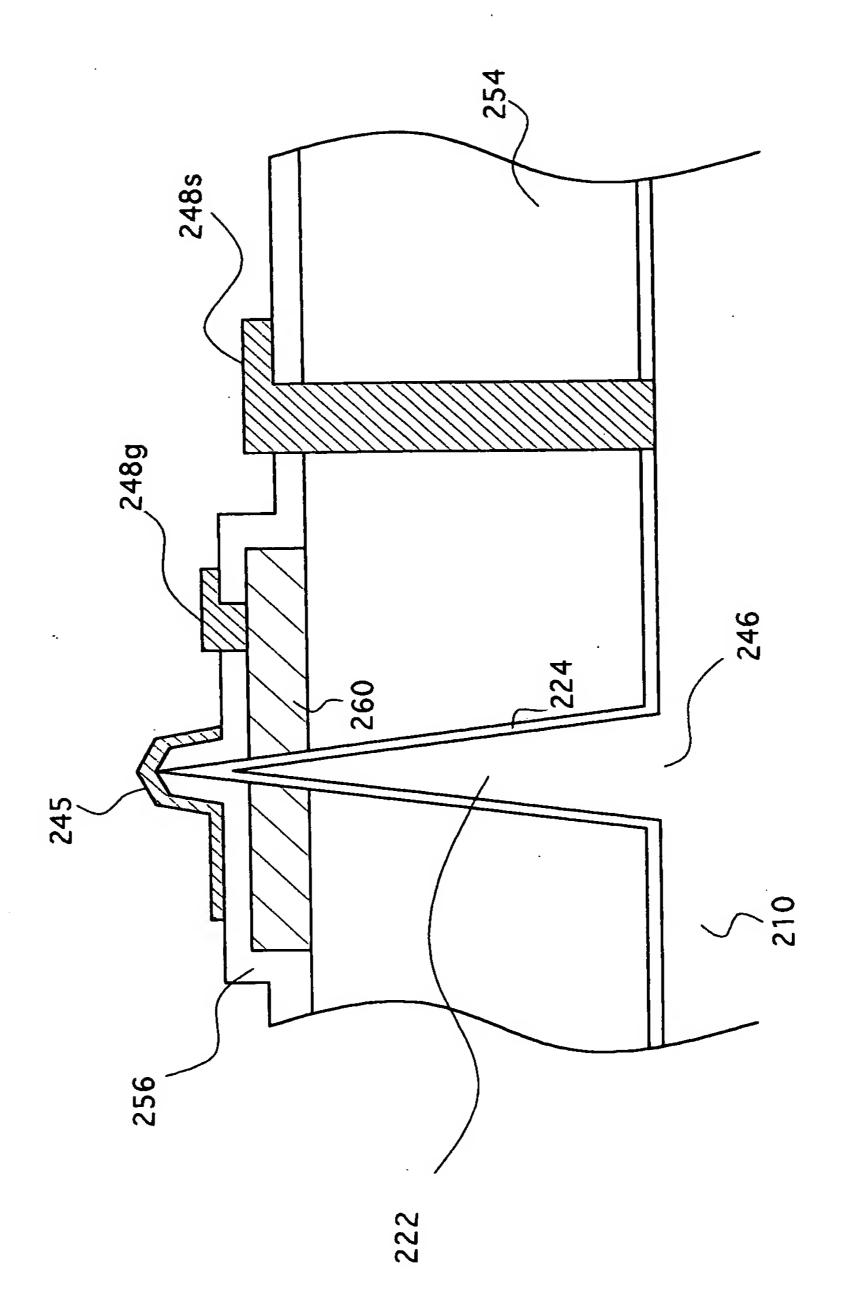
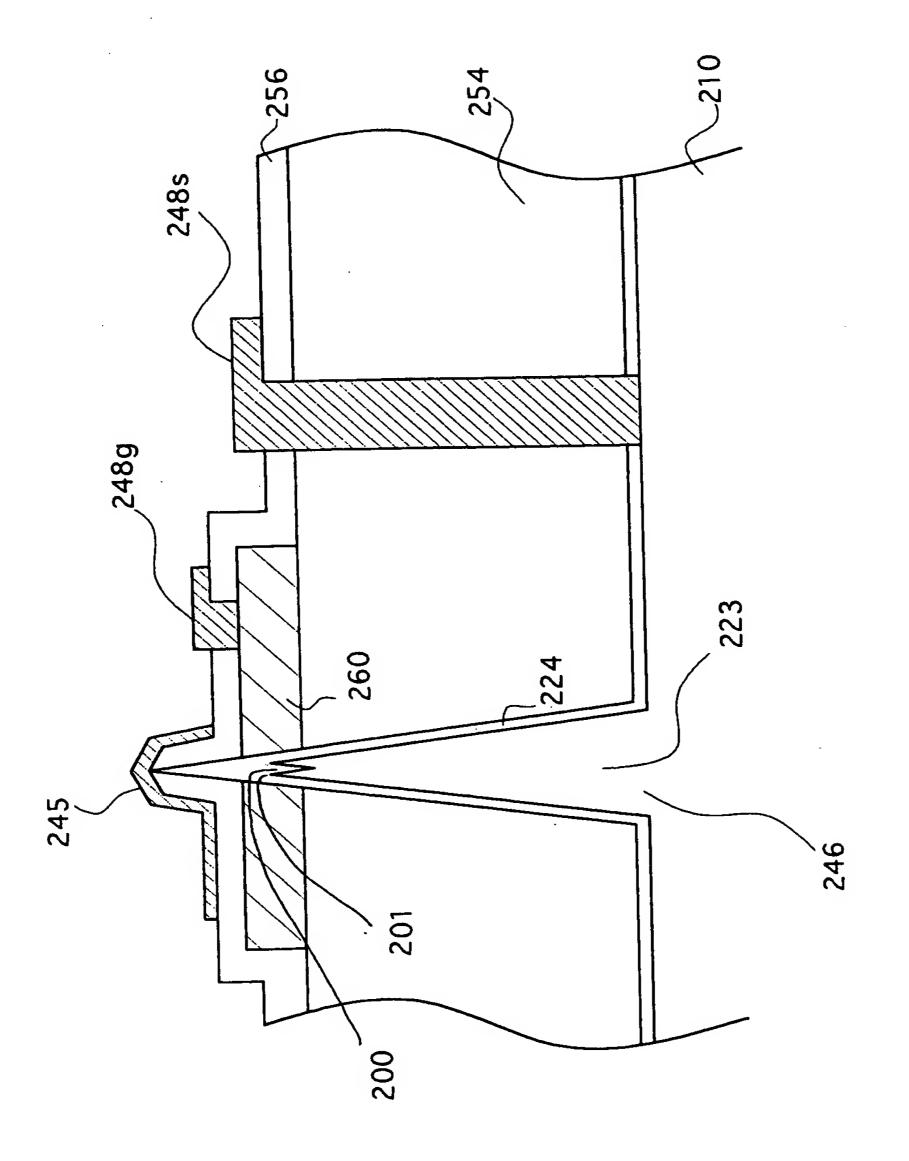
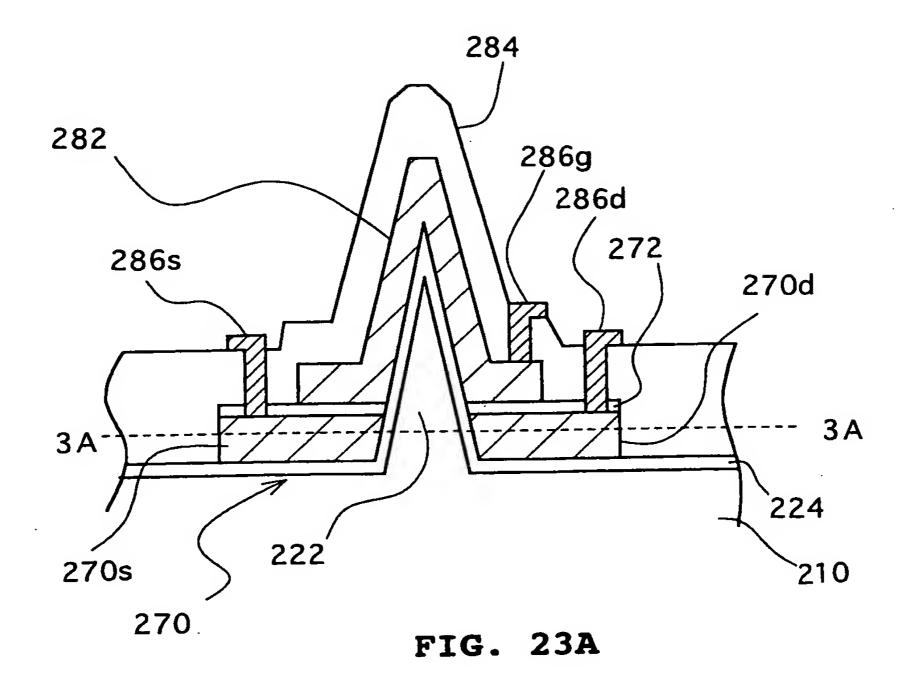


FIG. 21



'IG. 22



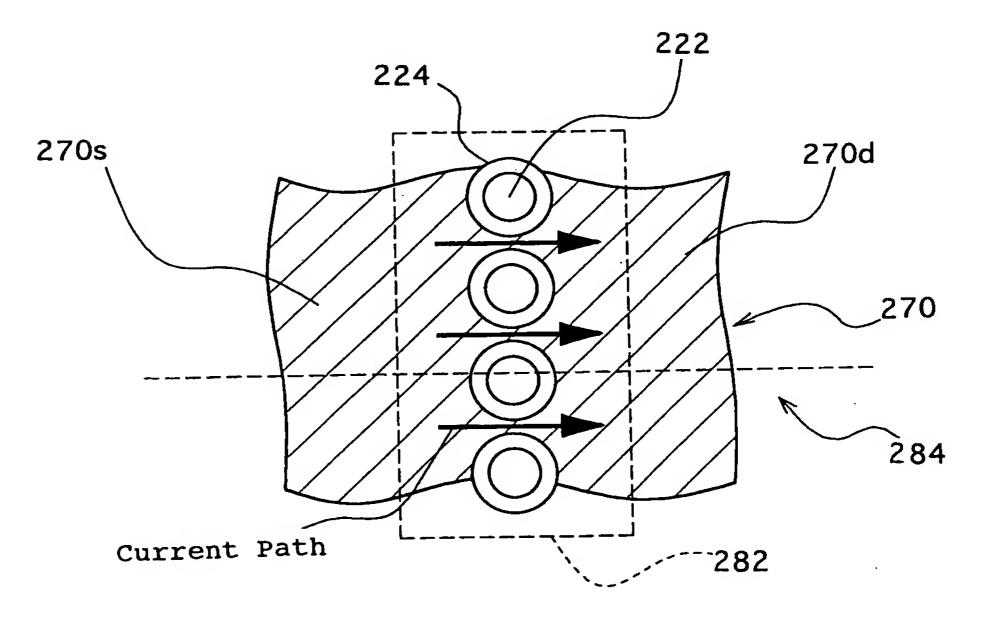


FIG. 23B

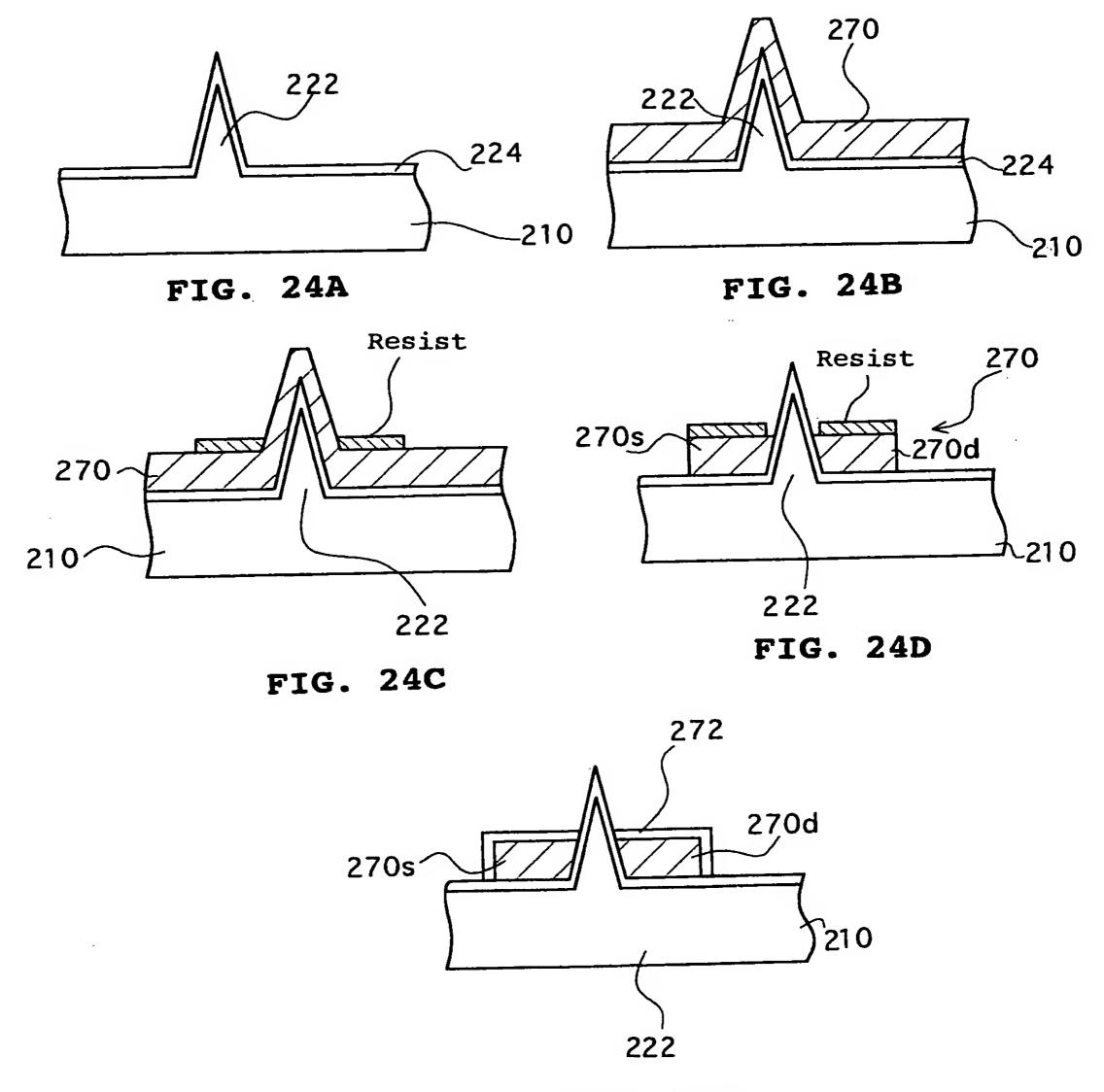
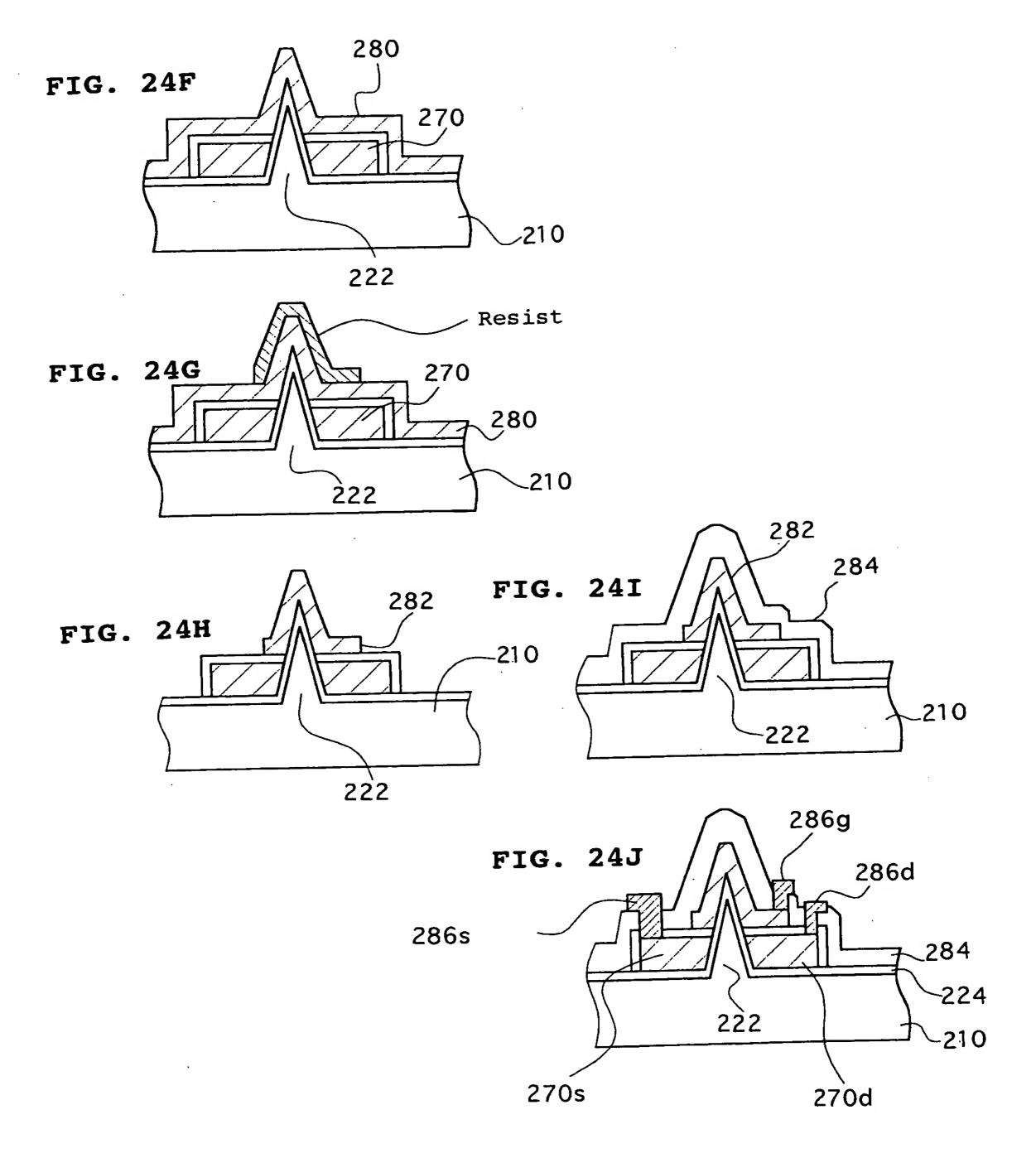


FIG. 24E



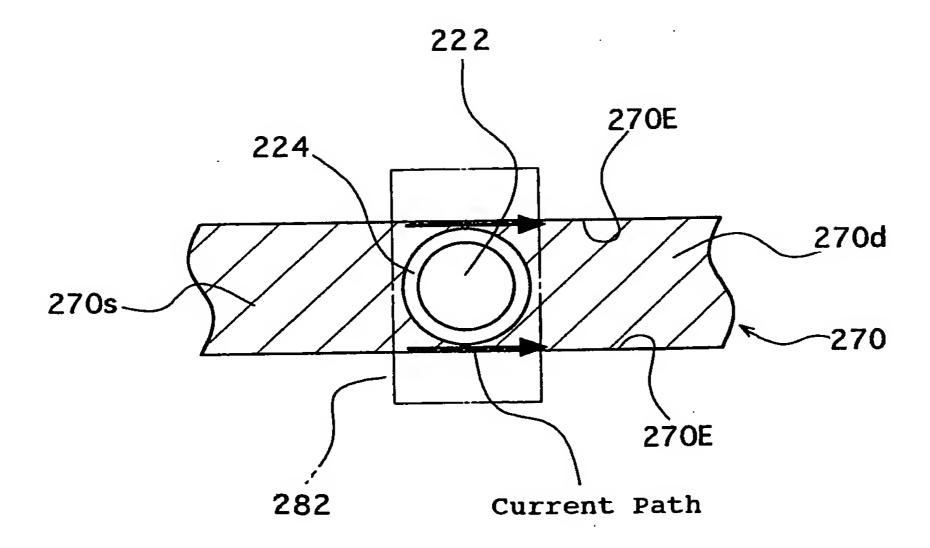


FIG. 25A

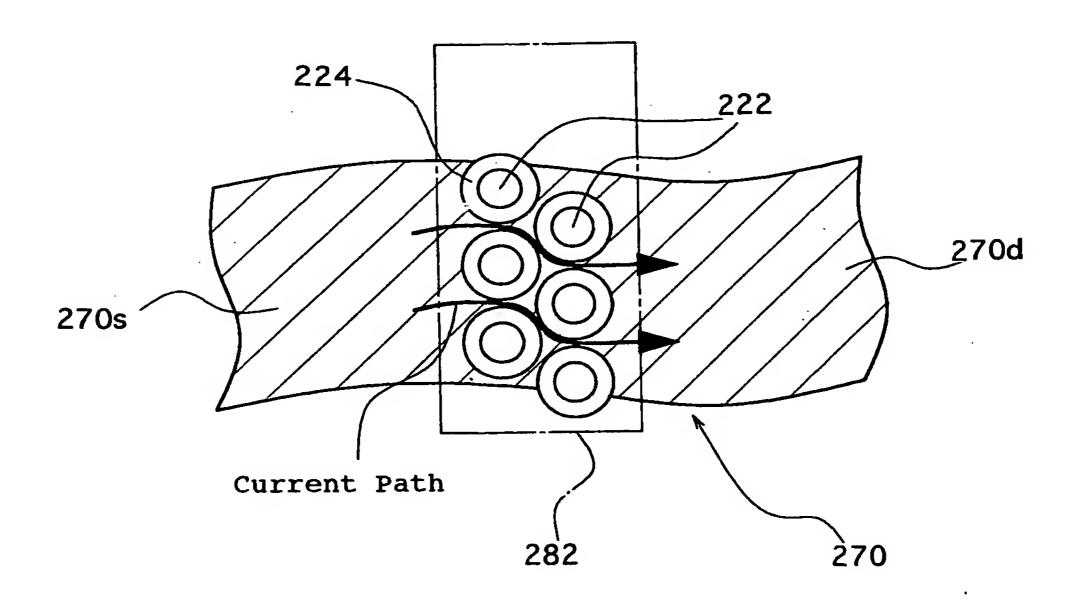


FIG. 25B

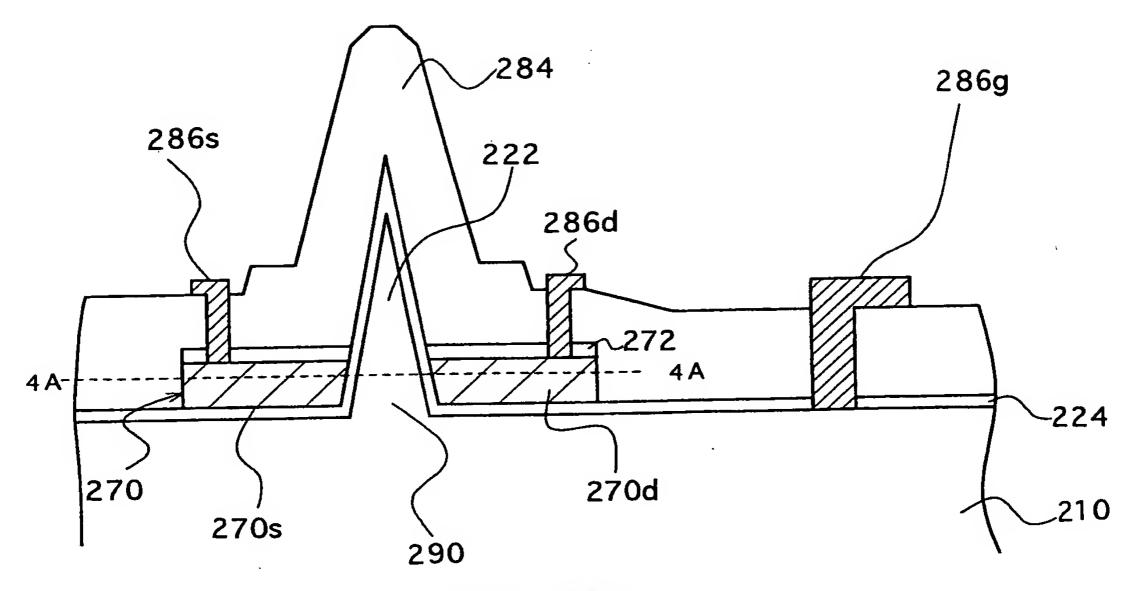


FIG. 26A

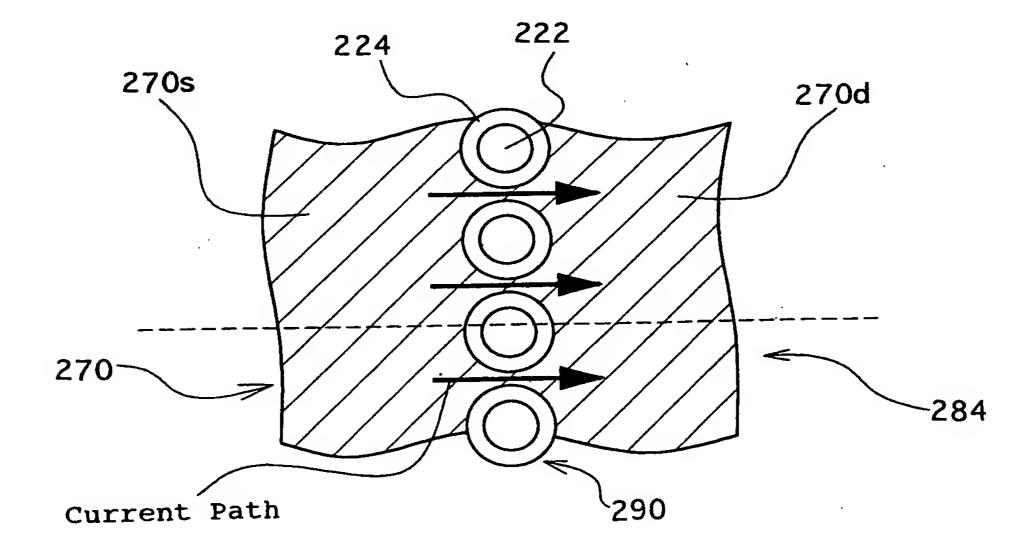


FIG. 26B

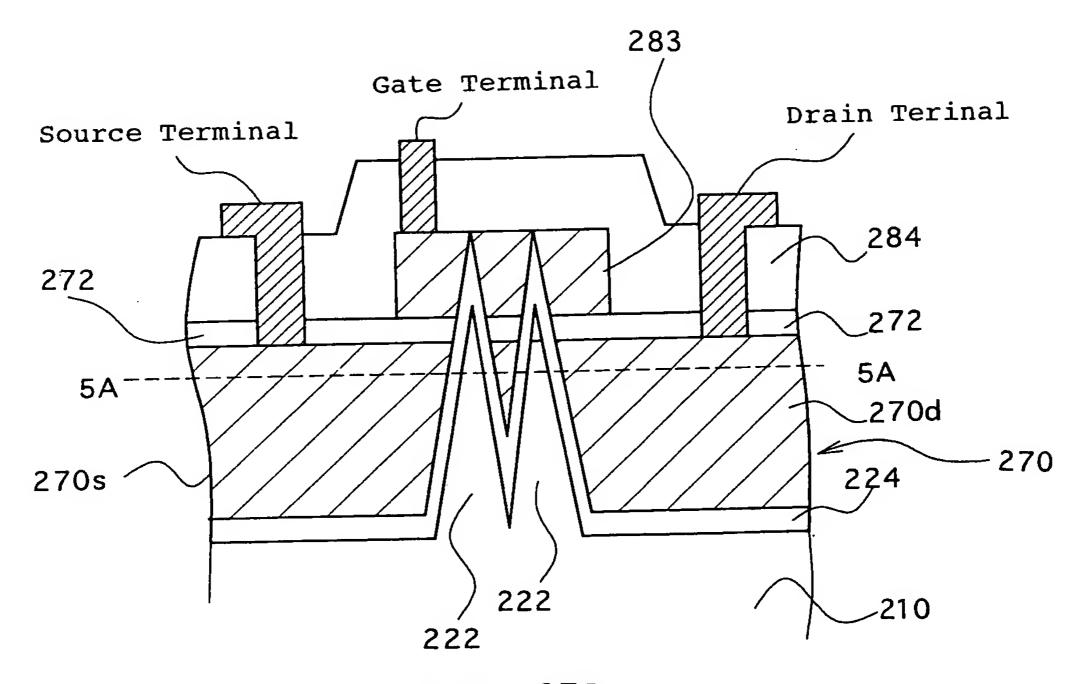


FIG. 27A

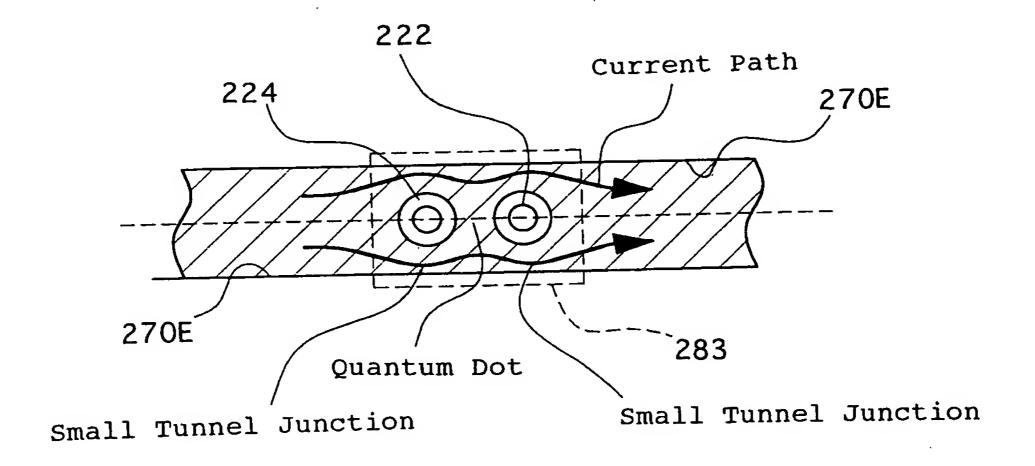


FIG. 27B

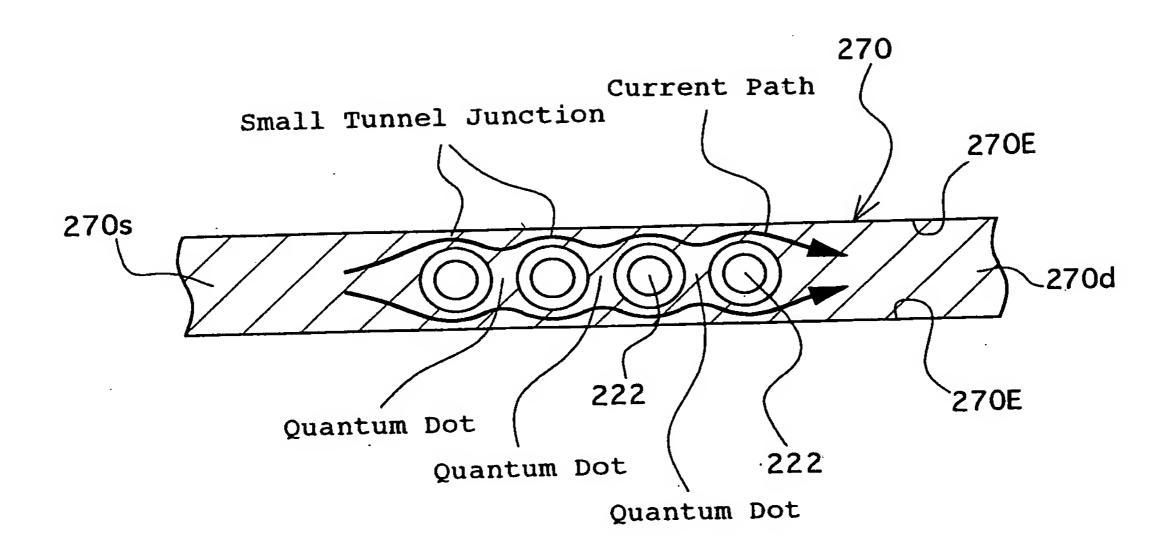


FIG. 28

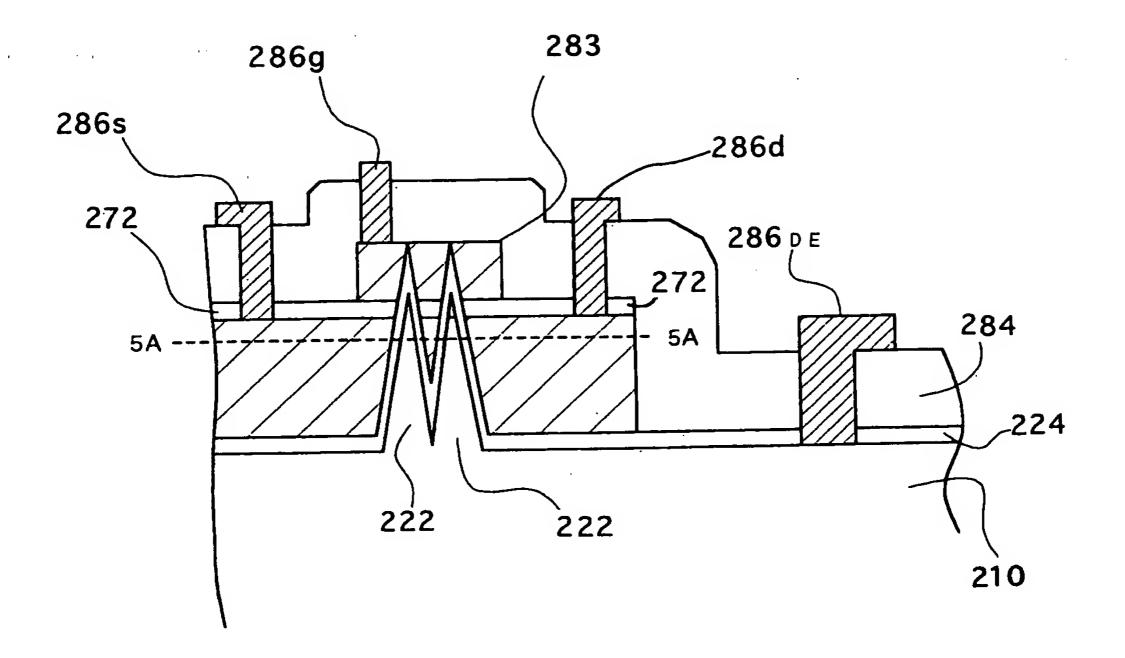


FIG. 29A

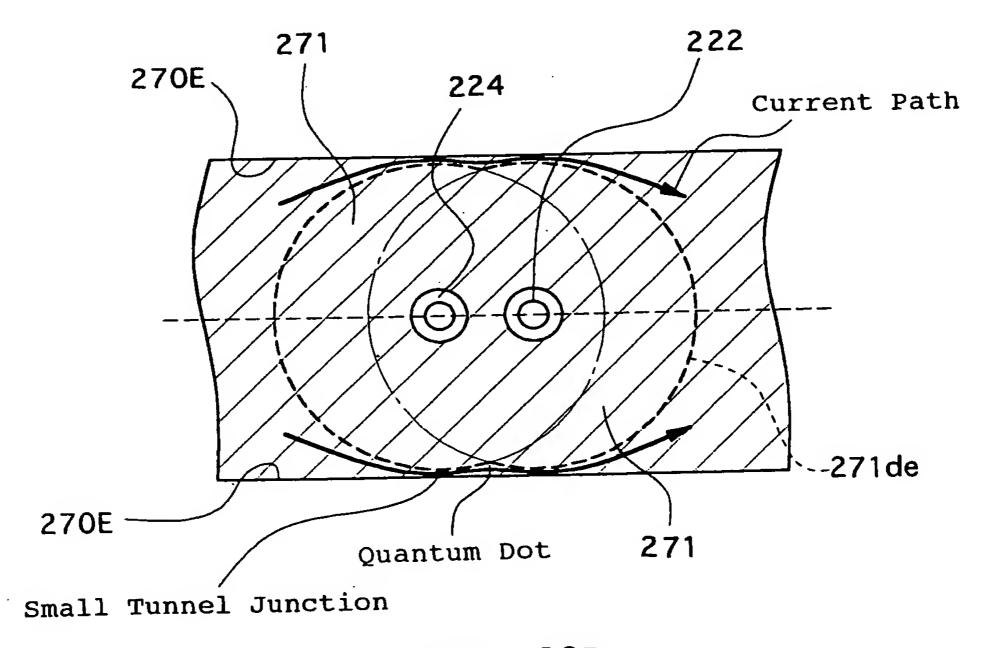


FIG. 29B

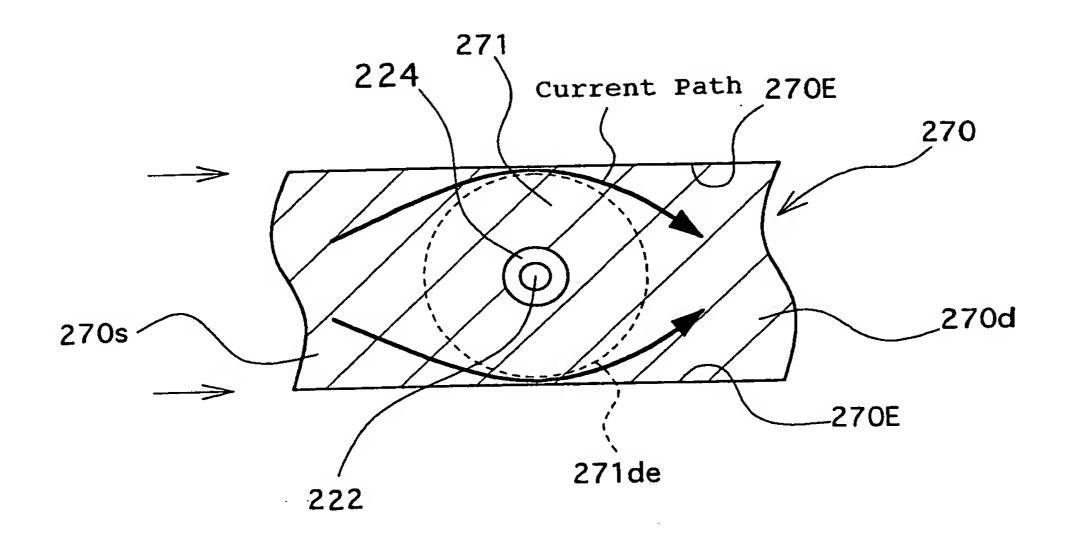


FIG. 30

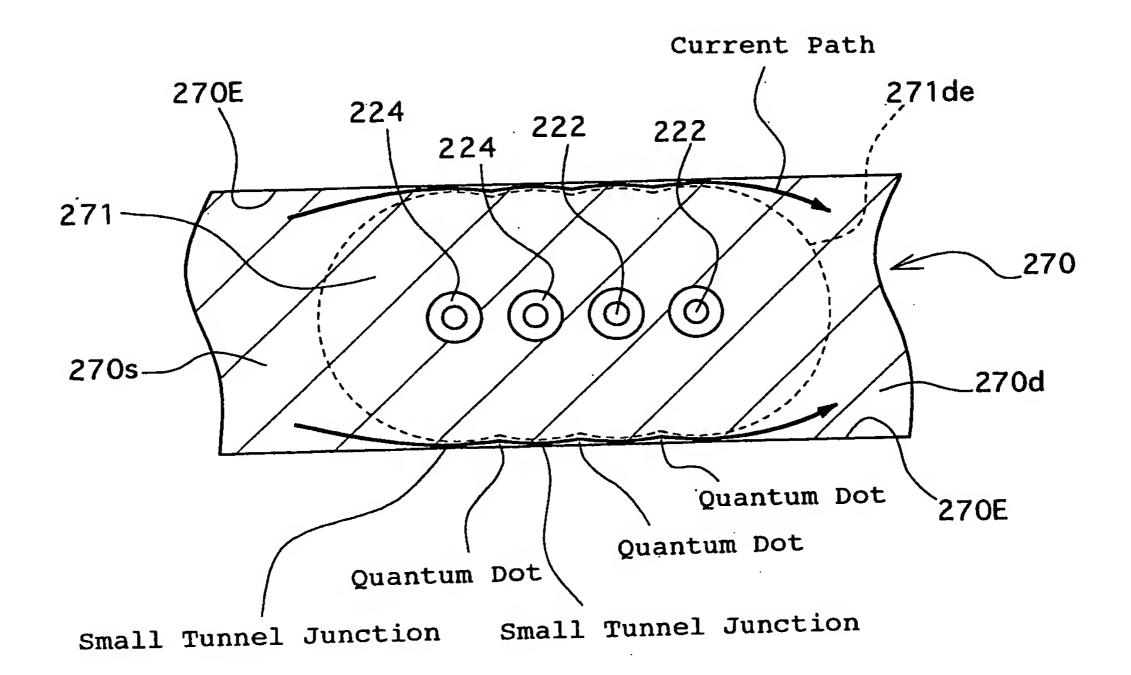


FIG. 31

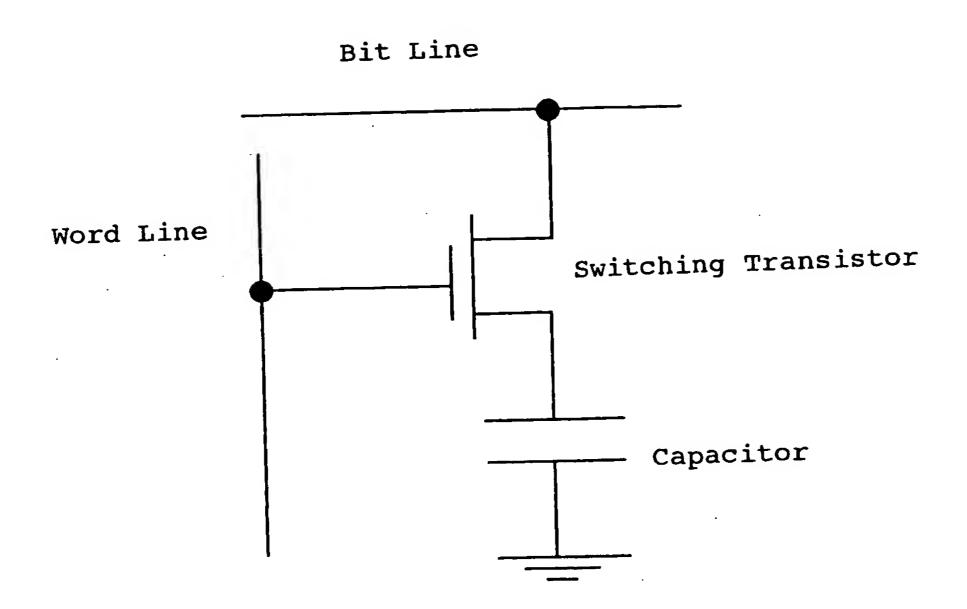


FIG. 32 PRIOR ART

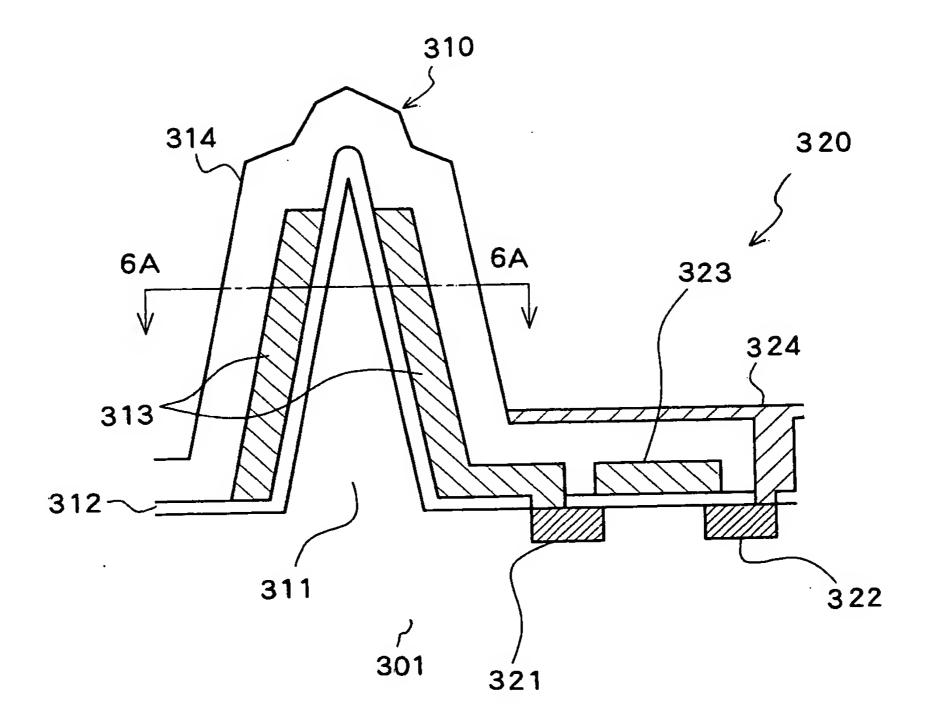


FIG. 33A

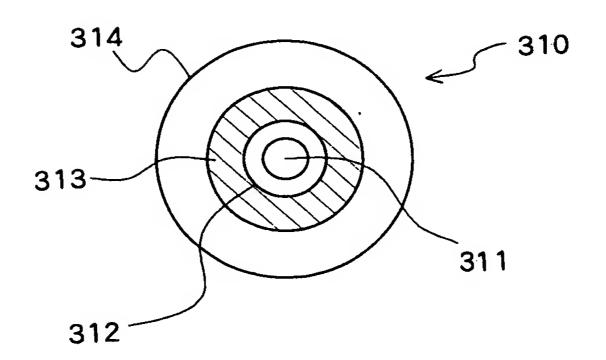


FIG. 33B

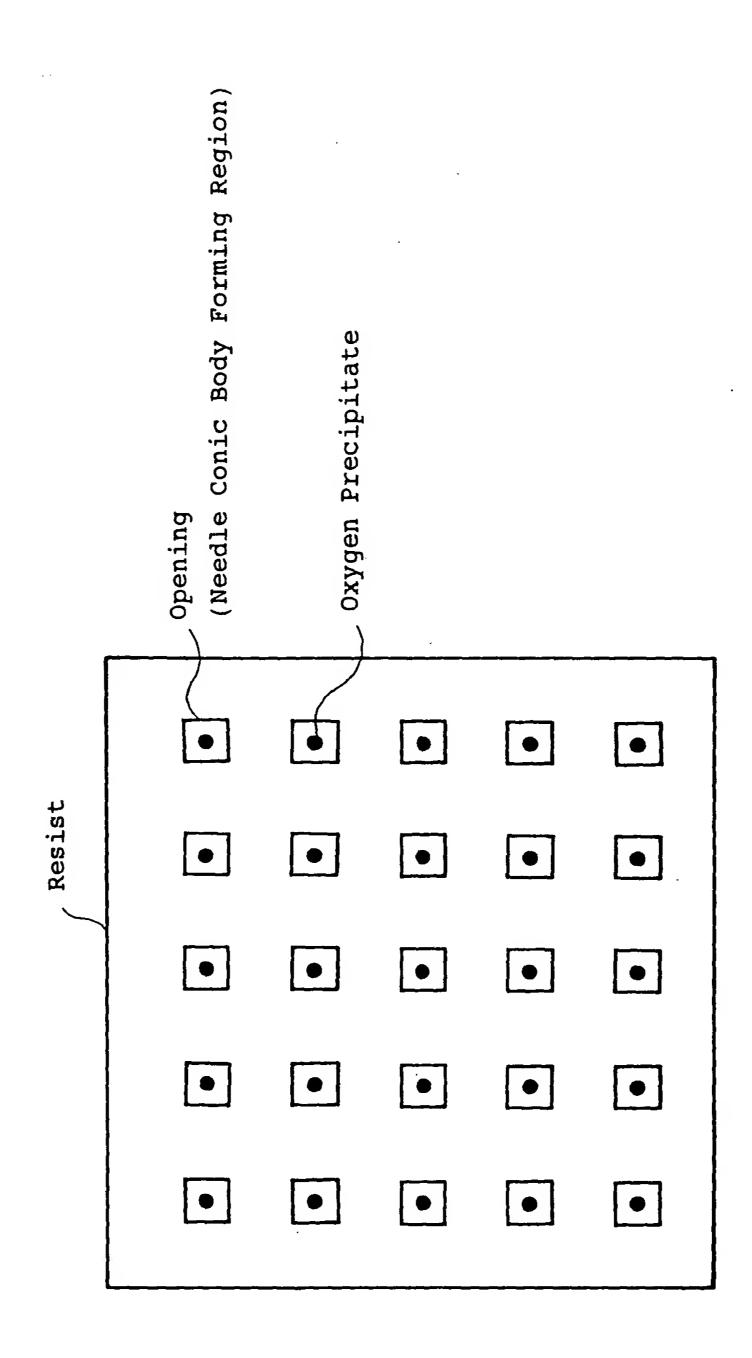
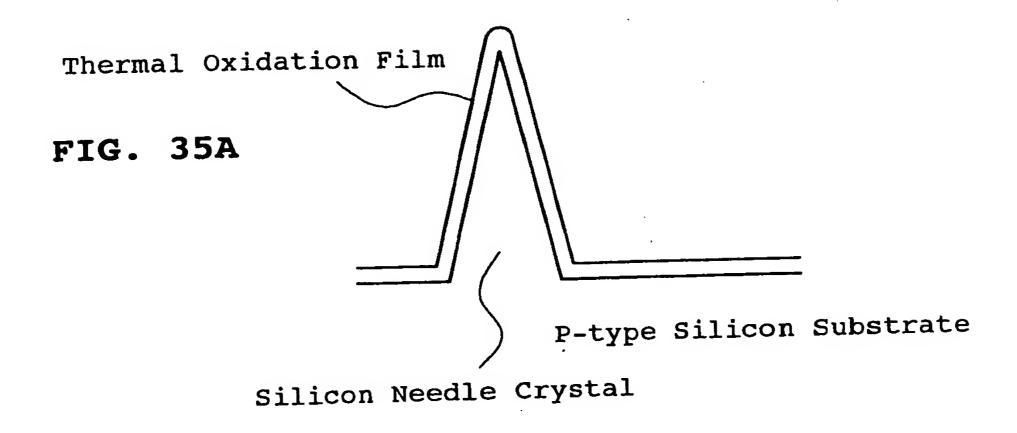
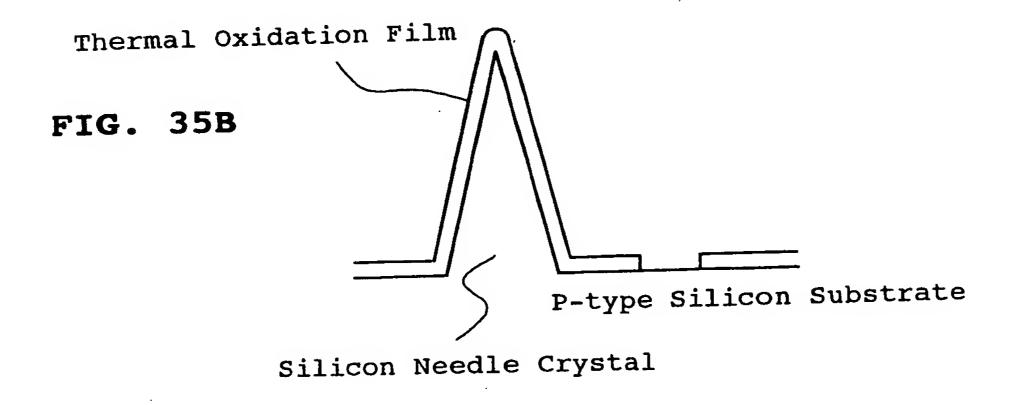
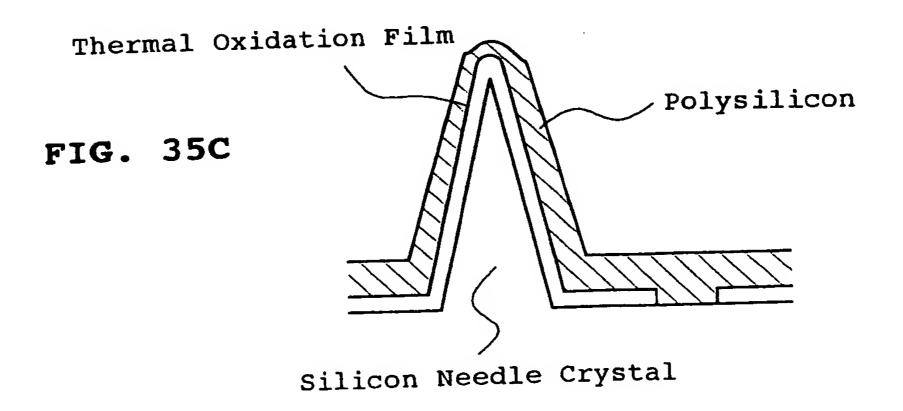
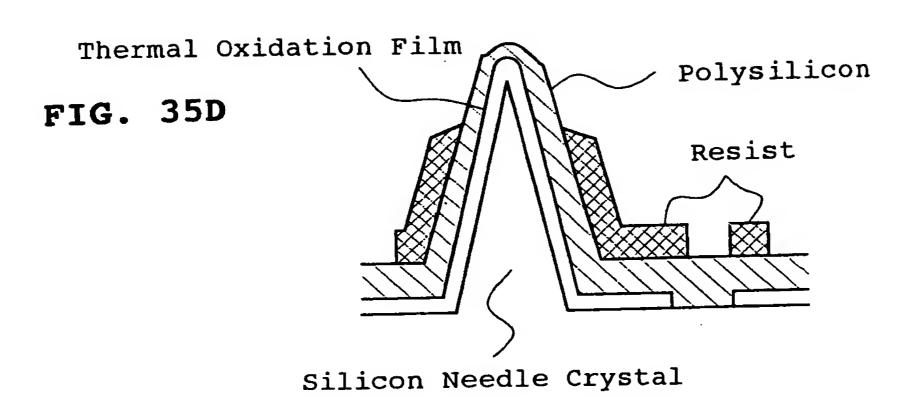


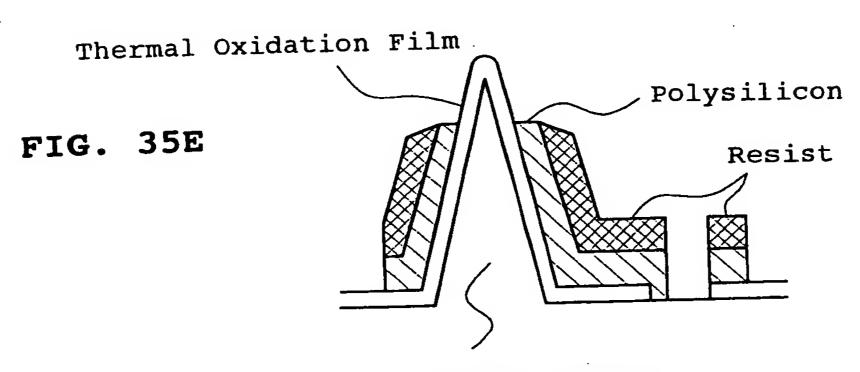
FIG. 34



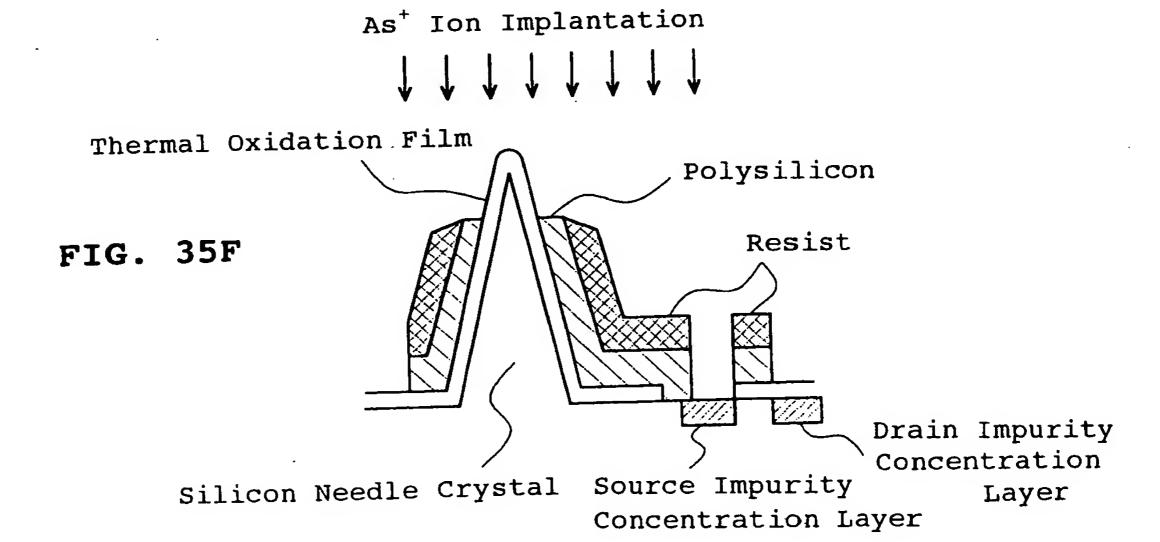








Silicon Needle Crystal



Oxide Film by CVD Method

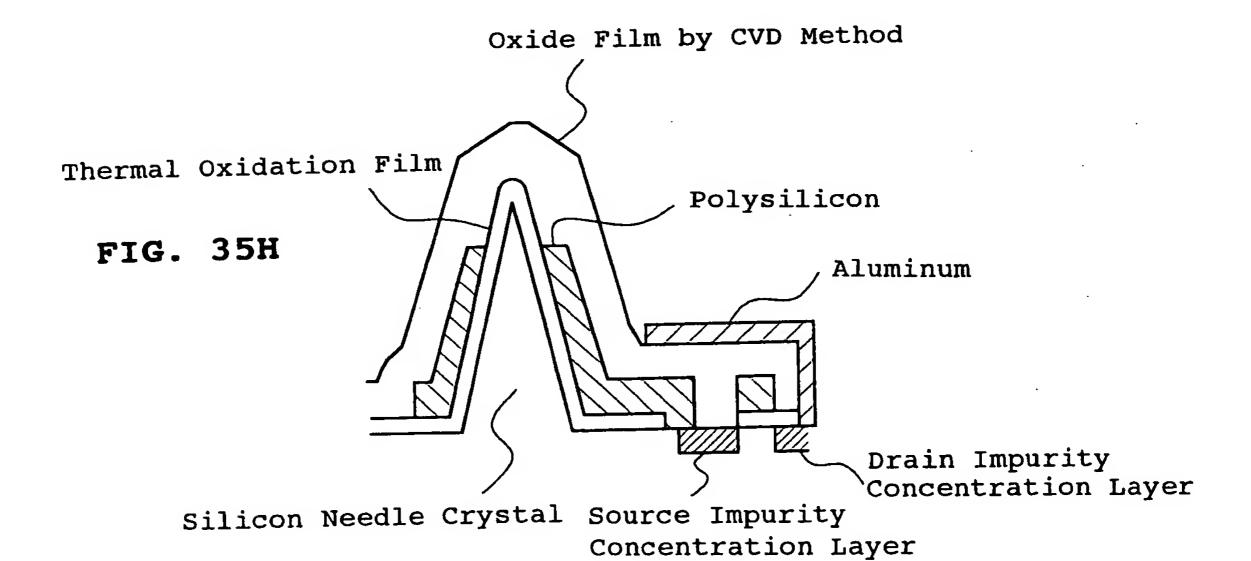
Thermal Oxidation Film

Polysilicon

FIG. 35G

Drain Impurity
Concentration Layer

Silicon Needle Crystal Source Impurity
Concentration Layer



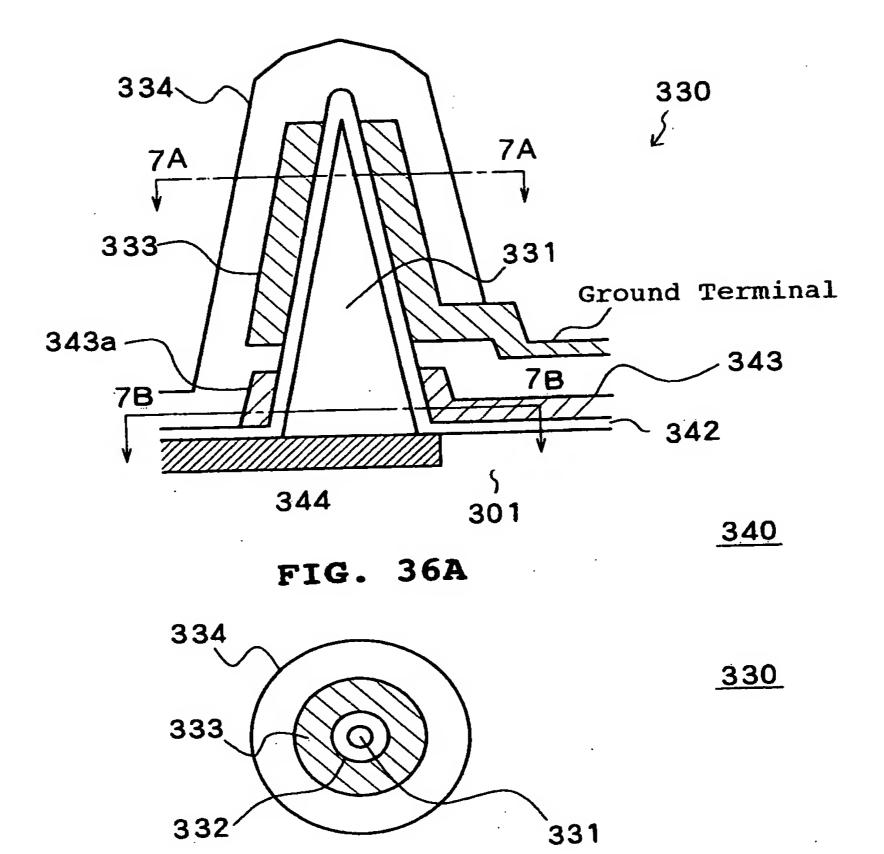


FIG. 36B

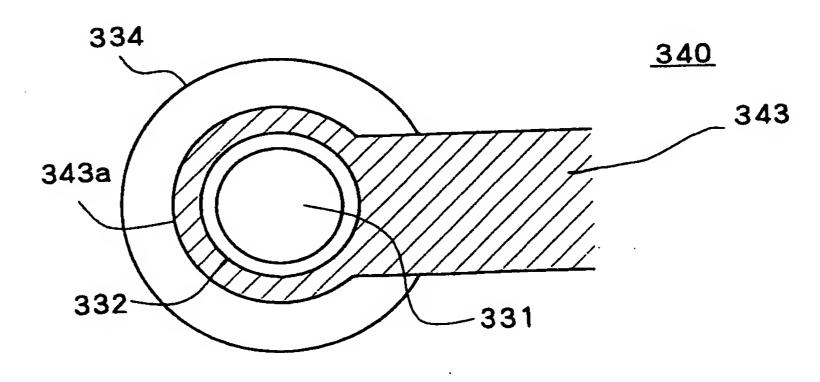
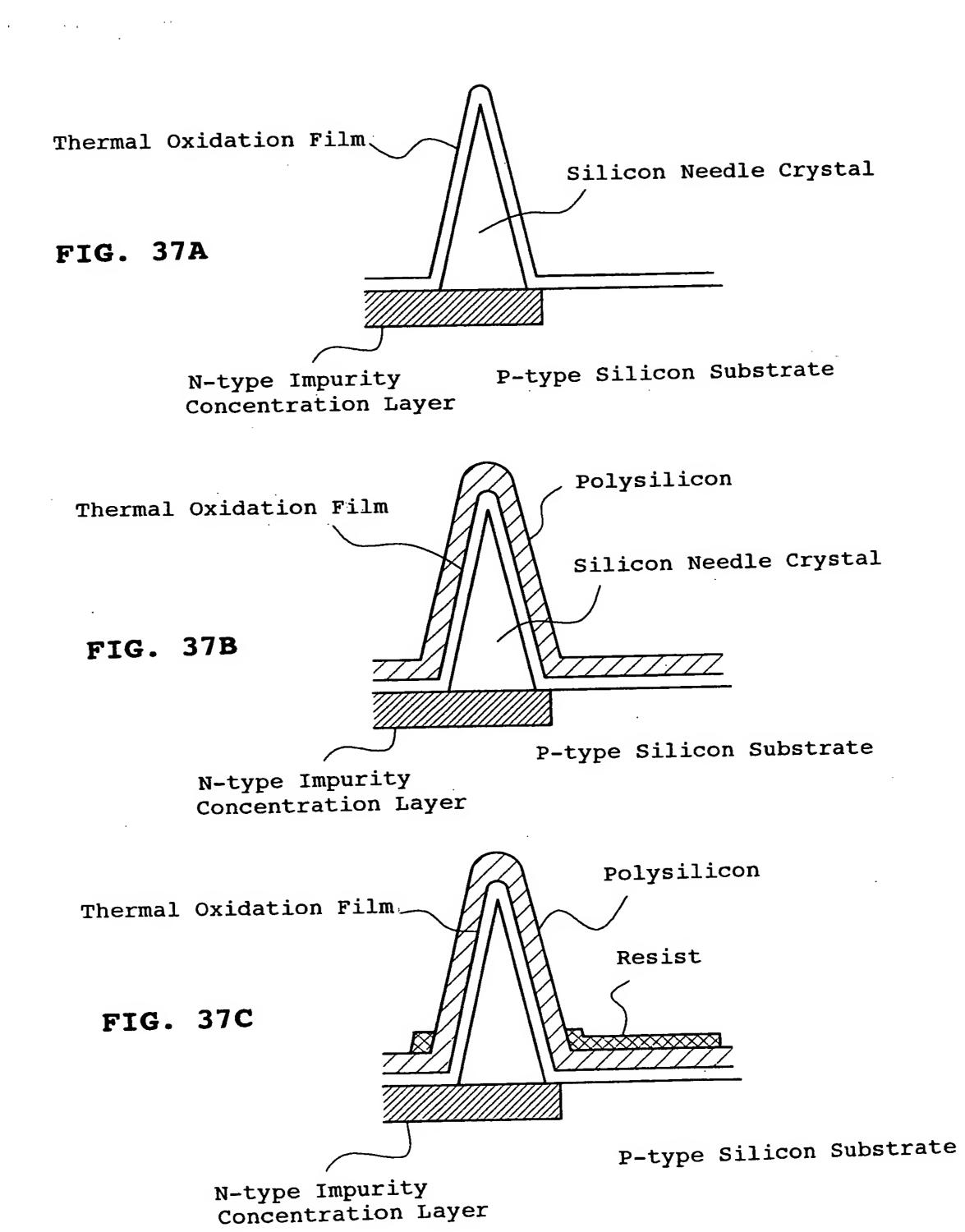
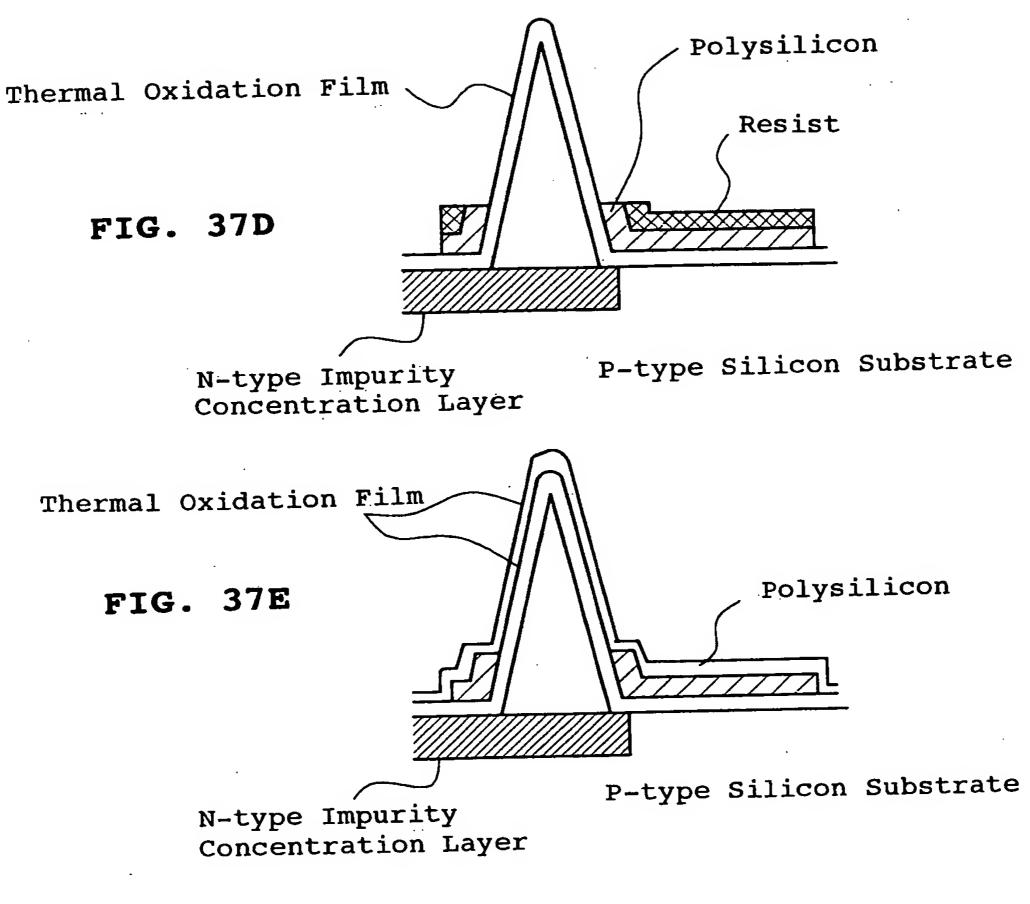
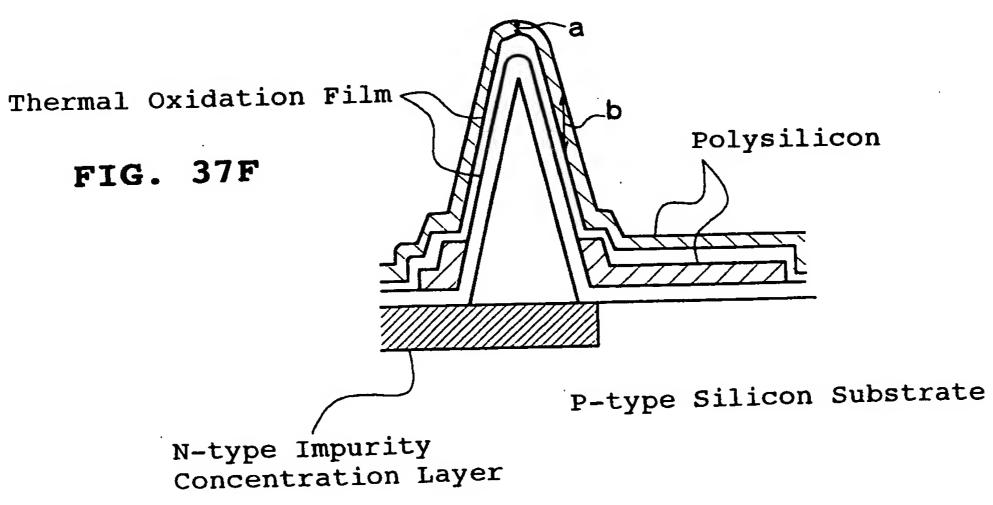
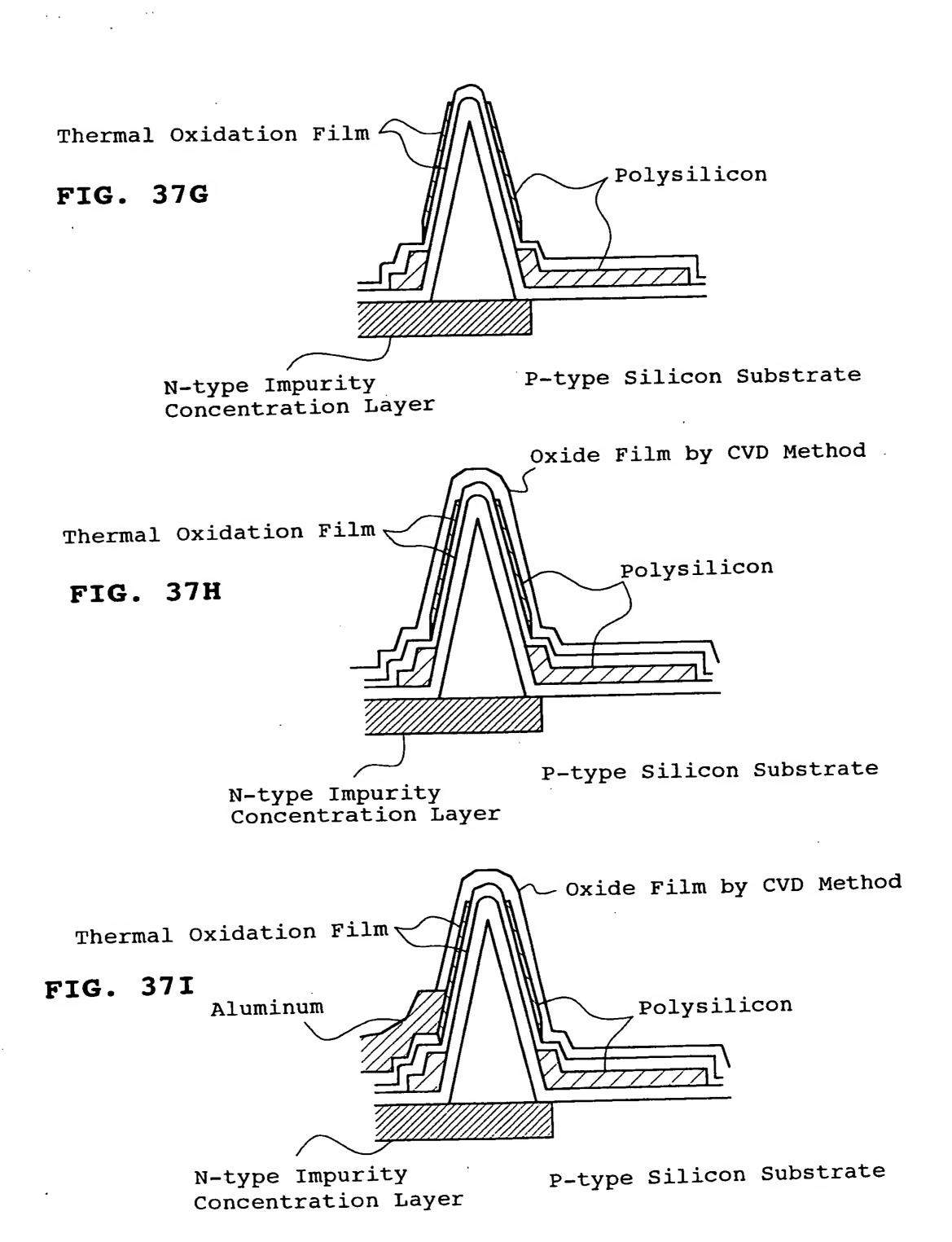


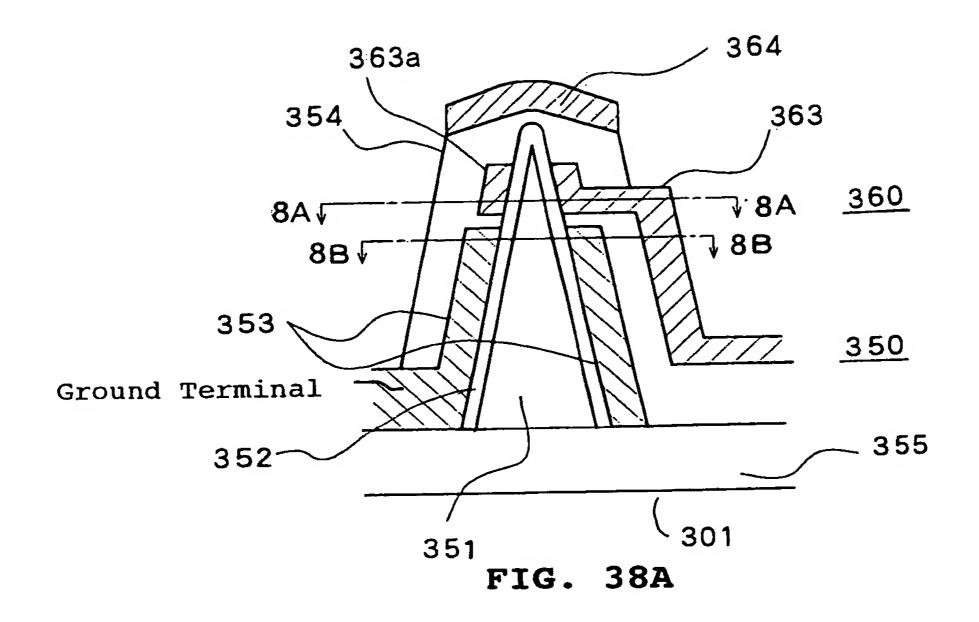
FIG. 36C











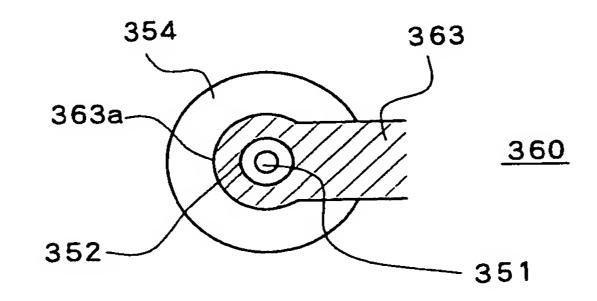


FIG. 38B

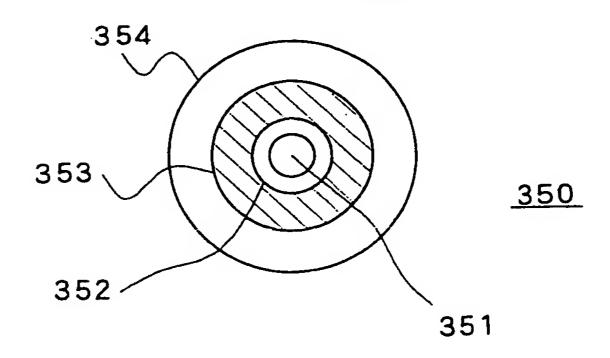


FIG. 38C

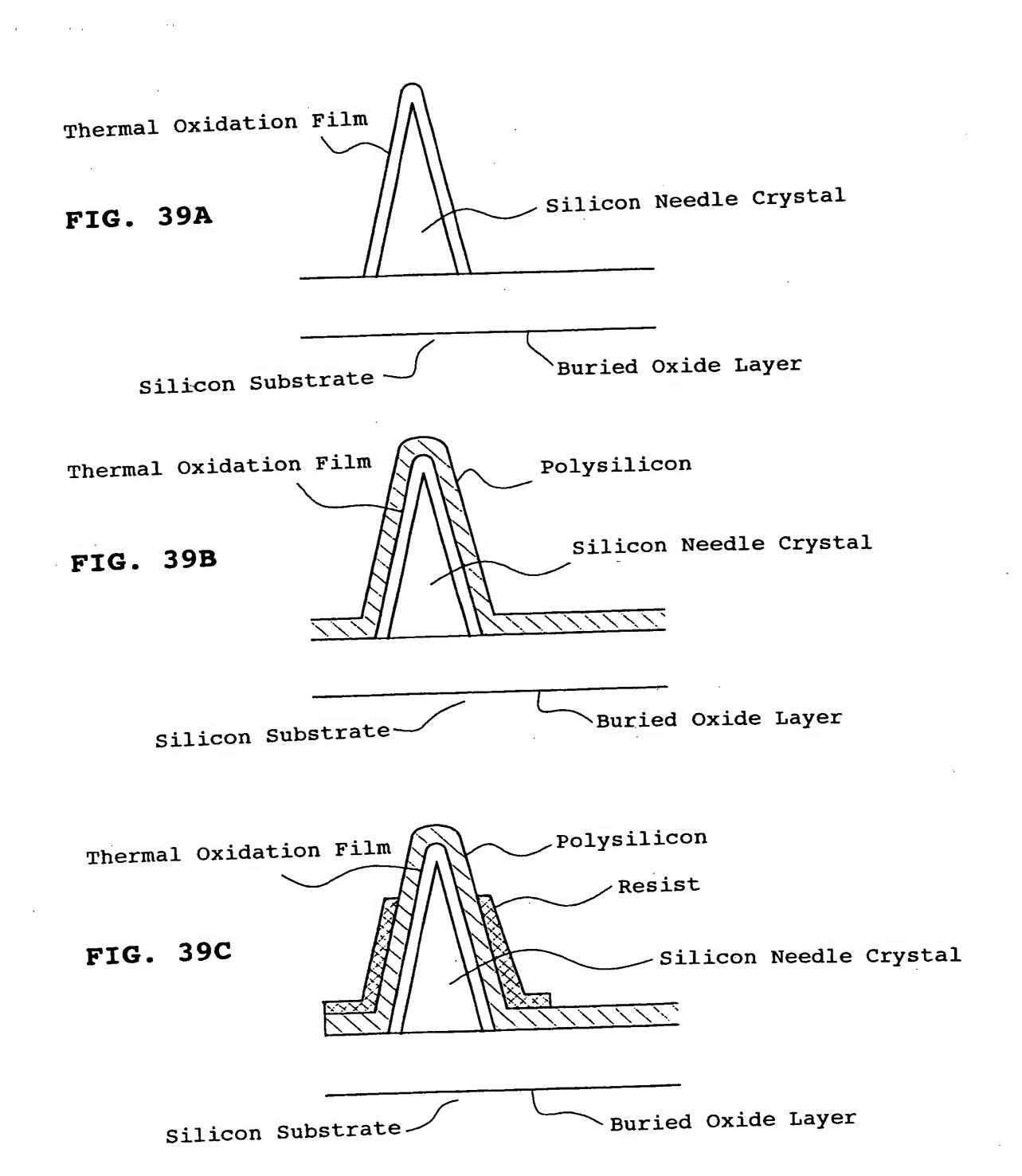


FIG. 39D

Silicon Substrate

Buried Oxide Layer

